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AAP11/AAP21

Schematic Document

SKL-H paltform with Nvidia N16E-GS/GT/GX

Rev: 1.0(A00) PVT

2015/07/21

@ : Nopop Component

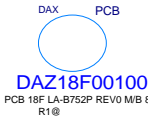
EMI@ /@EMI@ : EMI pop/unpop part
ESD@ /@ESD@ : ESD pop/unpop part
RF@ /@RF@ : RF pop/unpop part

CONN@ : Connector Component

AOAC@ : Intel AOAC
DS3/NODS3: deepS3
TBT@: ThunderBolt
PD@: Power Delivery

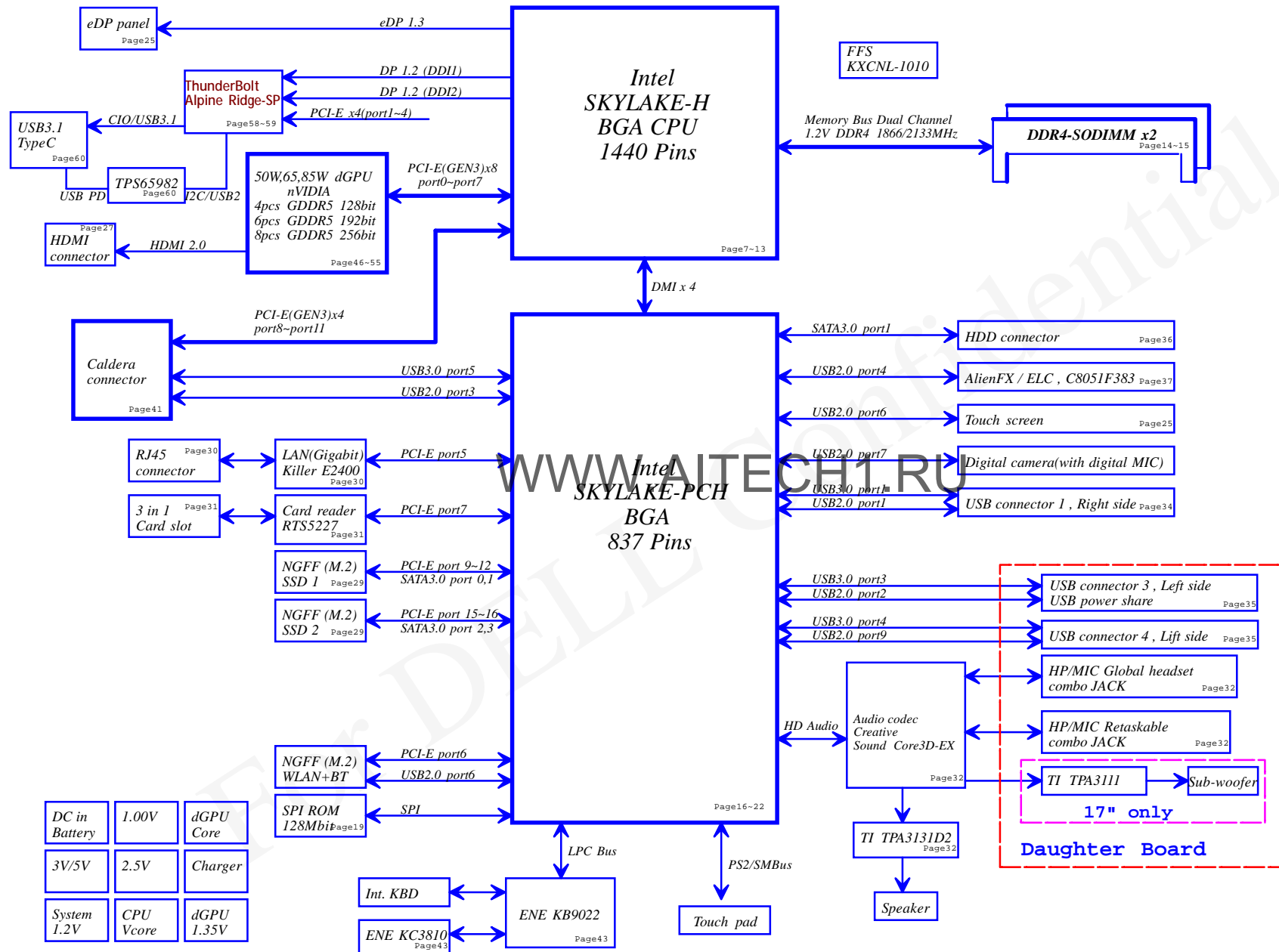
DIS@ : Discrete Part

N16EGS@:N16E-GS(2G)
N16EGT@:N16E-GT(3G)
N16EGX@:N16E-GX(4G)
2G@:2G VRAM
3G@:3G VRAM
4G@:4G VRAM



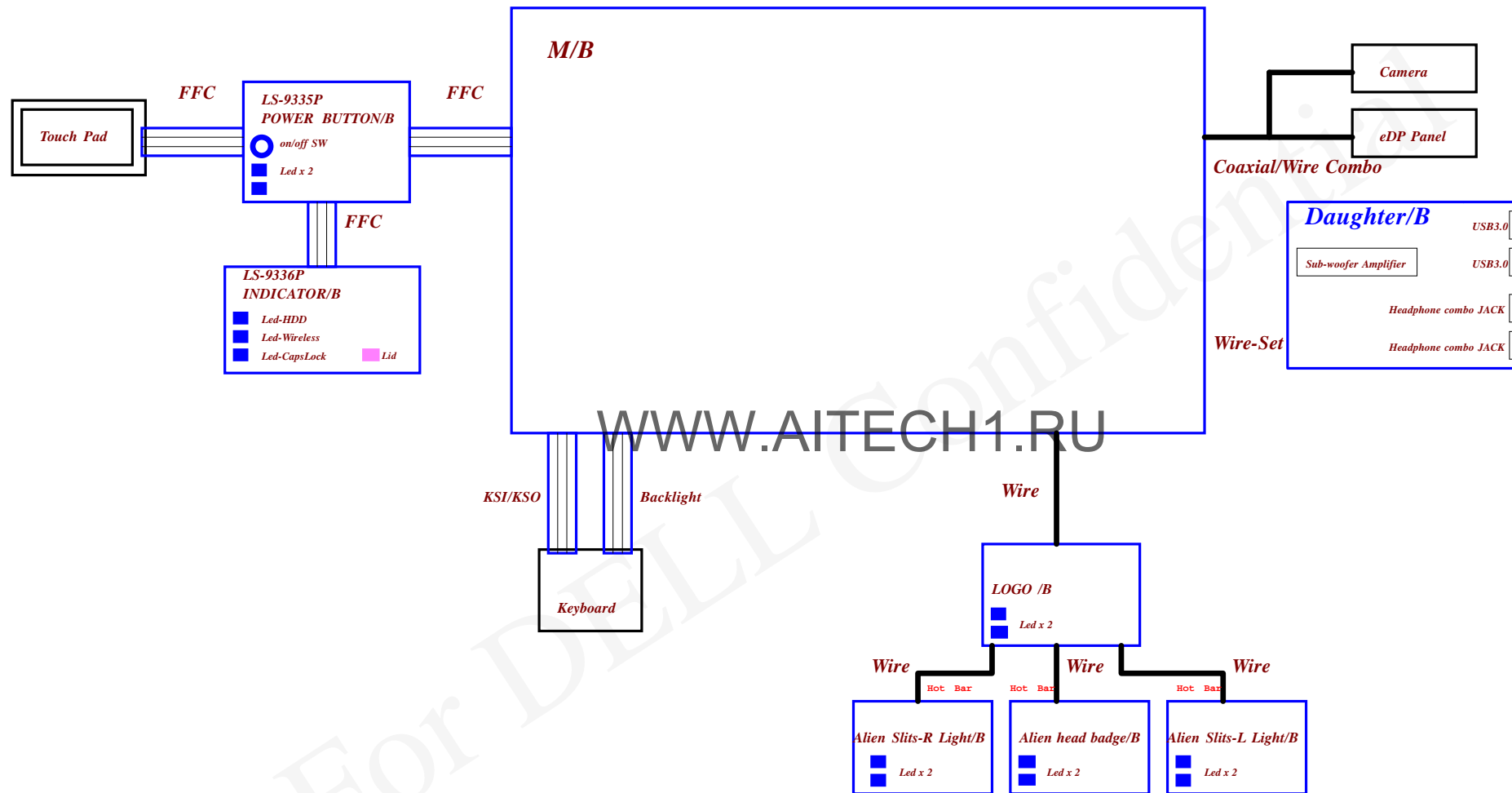
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				Date: Wednesday, July 22, 2015	Sheet 1 of 78

SKL+NV Block Diagram



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				Rev	0.1
				Sheet	2 of 78

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Size		Document Number			Rev
Date: Wednesday, July 22, 2015		Sheet 3 of 78			0.1

Board ID Table for AD channel

Vcc	3.3V +/- 1%					
Ra	100K +/- 1%					
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max	EC AD3	
0	0	0.000V	0.000V	0.300V	0x00 - 0x0B	NVIDIA Graphic
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C	
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26	
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30	
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3B	
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3C - 0x46	
6	43K +/- 1%	0.978V	0.992V	1.006V	0x47 - 0x54	
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64	
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76	
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87	
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96	AMD Graphic
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA3	
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA4 - 0xAD	
13	240K +/- 1%	2.316V	2.329V	2.343V	0xAE - 0xB7	
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xC0	
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC1 - 0xC9	
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD3	
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD4 - 0xDC	
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDD - 0xE6	
19	NC	3.000V	3.300V	3.300V	0xE7 - 0xFF	

Board ID TABLE

ID	PCB Revision
NV	AMD
0	10
1	11
2	12
3	13
4	14
5	15

TBT connector change to SMD type.

Symbol Note :



: means Digital Ground



: means Analog Ground

CLOCK SIGNAL	
CLKOUT_PCIE0	
CLKOUT_PCIE1	
CLKOUT_PCIE2	10/100/1000 LAN
CLKOUT_PCIE3	M.2 Card WLAN
CLKOUT_PCIE4	dGPU (N16)
CLKOUT_PCIE5	DGPU (Caldera)

USB3.0

Port1	Right side1
Port2	Right side2
Port3	Left side 1
Port4	
Port5	Caldera
Port6	Left side 2

USB2.0

Port0	Right side1
Port1	Left side 1 (PowerShare)
Port2	Caldera
Port3	ELC
Port4	BT
Port5	Touch screen
Port6	Camera
Port7 / 8	Right side 2 Left side 2

PCI EXPRESS

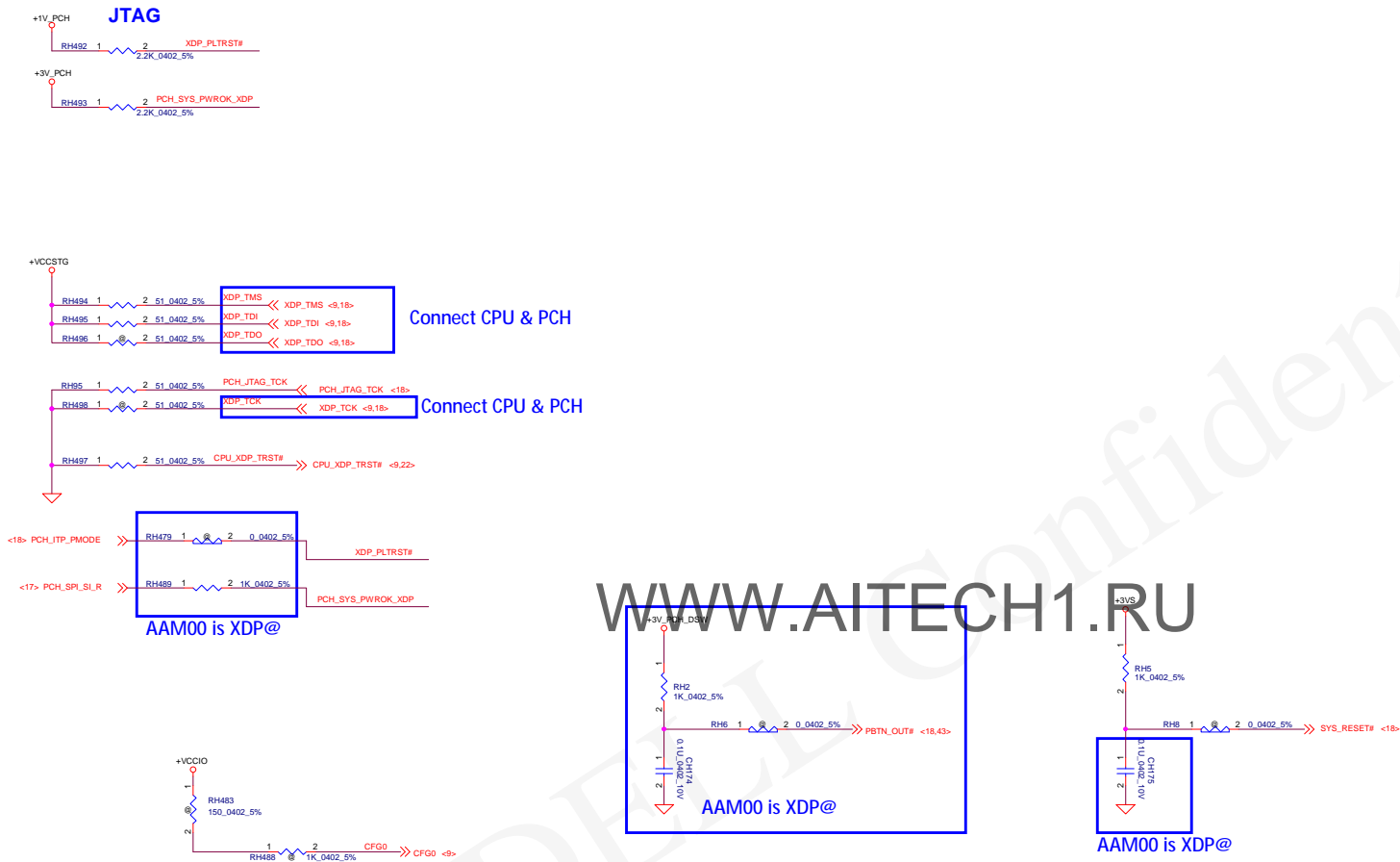
Lane 1	
Lane 2	
Lane 3	10/100/1000 LAN
Lane 4	M.2 Card WLAN
Lane 5	PCIE 4x MUX
Lane 6	

SATA

SATA0	HDD
SATA1	NGFF SSD
SATA2	NGFF SSD
SATA3	

BDW

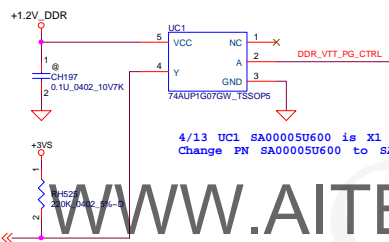
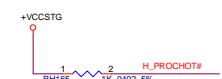
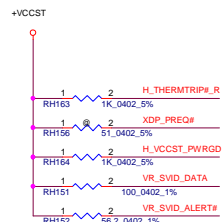
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					LA-C912P	0.1
				Date	Wednesday, July 22, 2015	Sheet 4 of 78



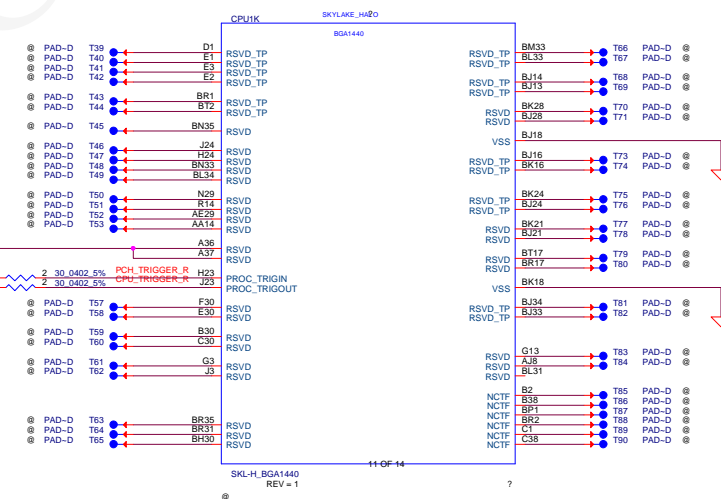
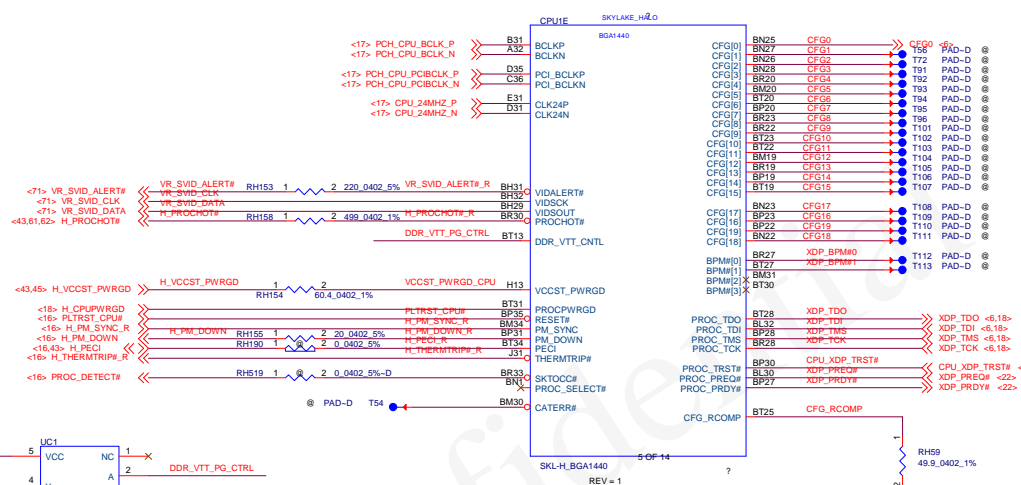
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Size	Document	Number	Rev	0.1
Date:	Wednesday, July 22, 2015	Sheet	6	of 78



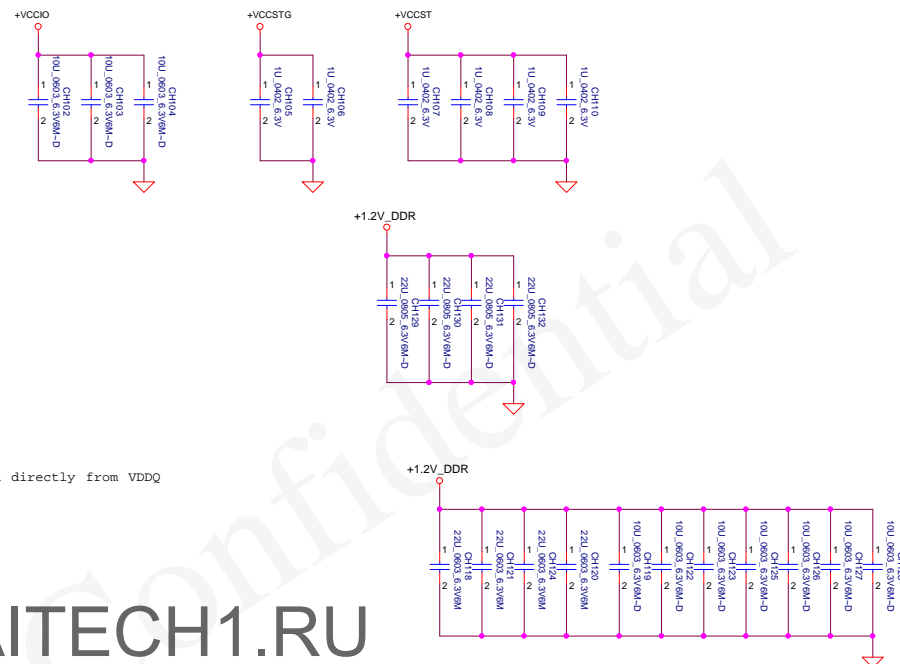




4/13 UC1 SA00005U600 is X1 code.
Change PN SA00005U600 to SA00007WE00.

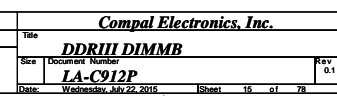


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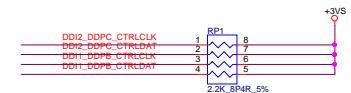
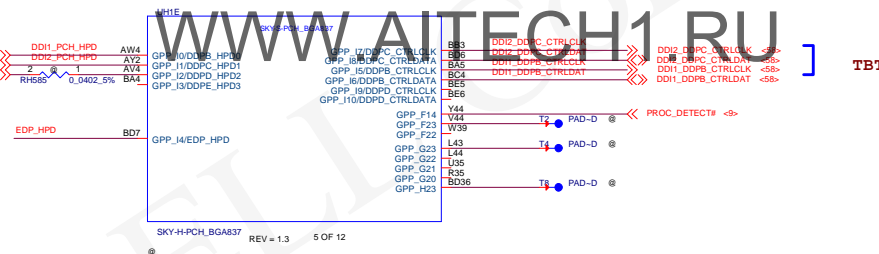
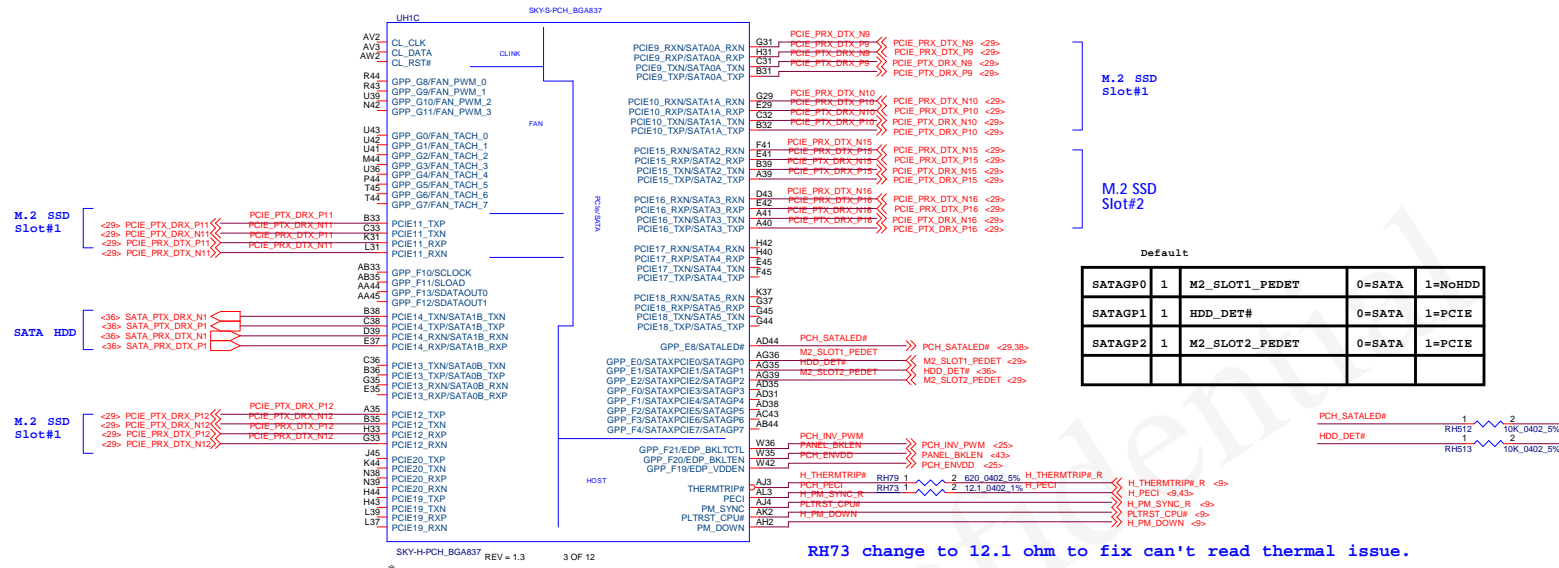
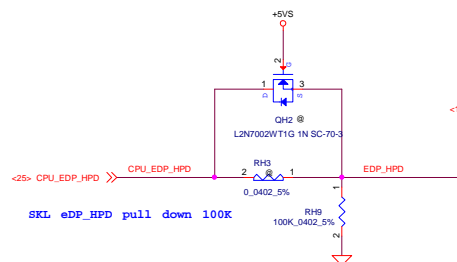


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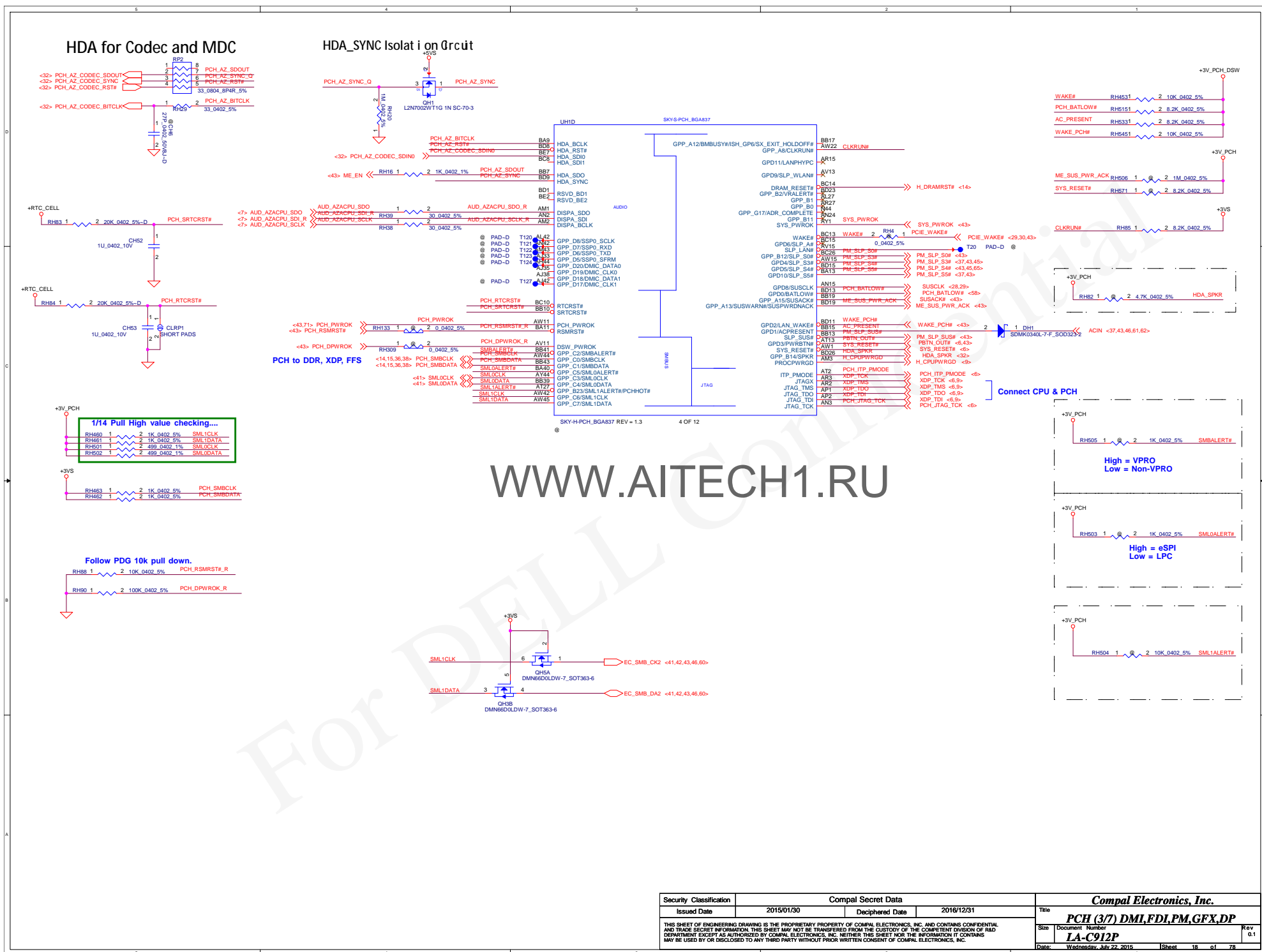


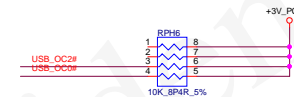
PCH Strap PIN

DisplayPort* Disabling and Termination Guidelines

Port	Strap	How to Enable Port?	How to Disable Port?
Port B	DOPB_CTRLDATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect
Port C	DOPC_CTRLDATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect
Port D	DOPD_CTRLDATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect

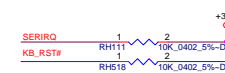
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					LA-C912P
				Date	Wednesday, July 22, 2015
				Sheet	16 of 78



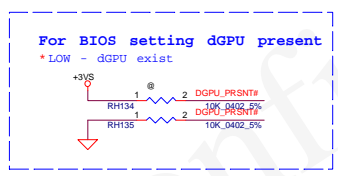


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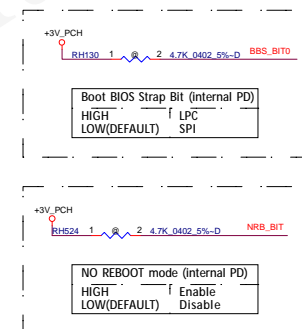
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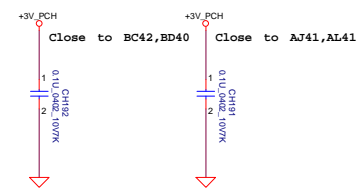
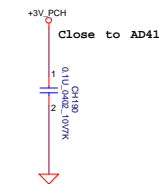
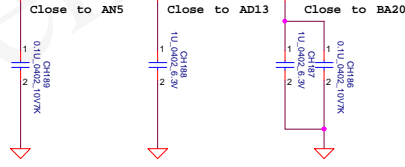
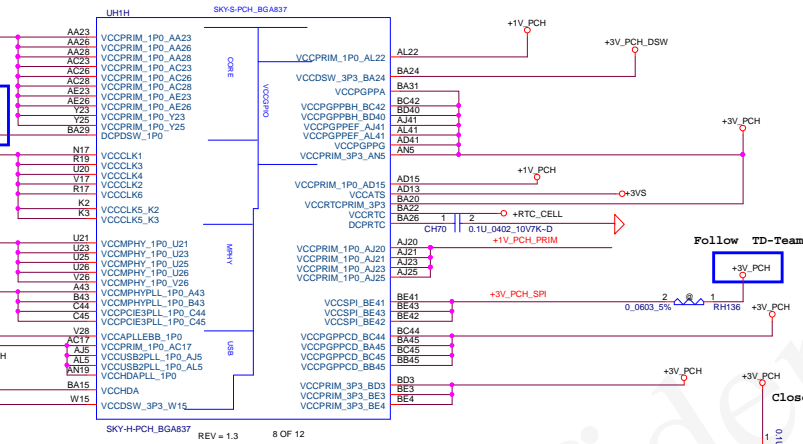
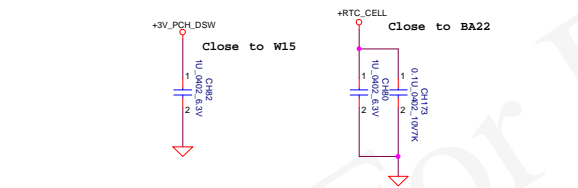
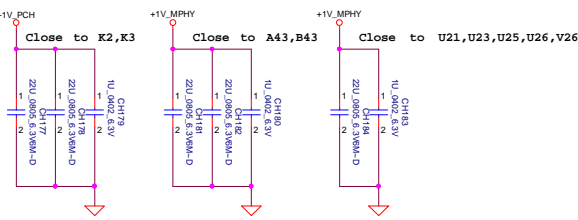
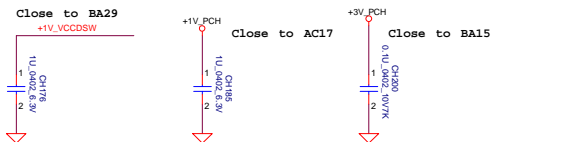
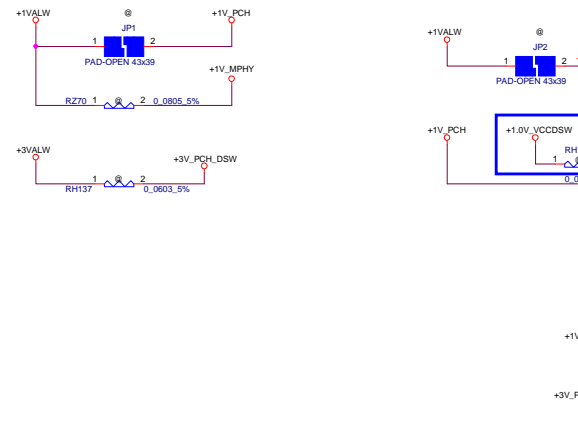
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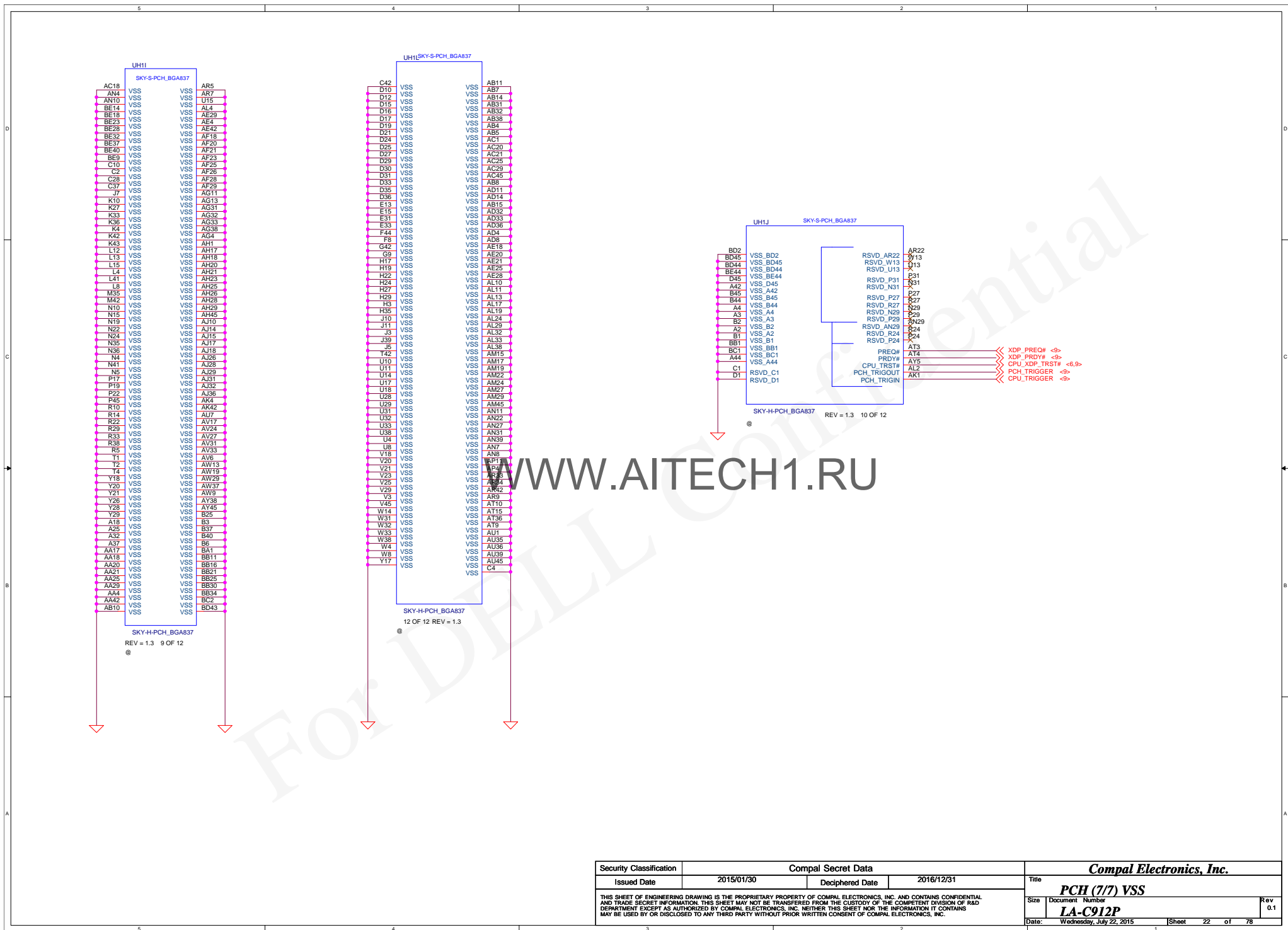
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				Sheet	21 of 78



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				Date:	Wednesday, July 22, 2015
				Sheet	22 of 78
				Rev	0.1

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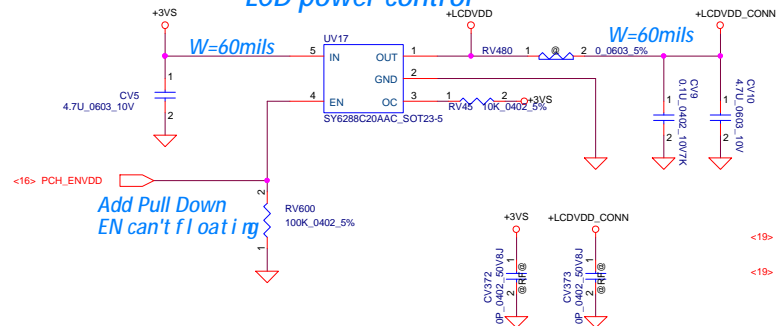
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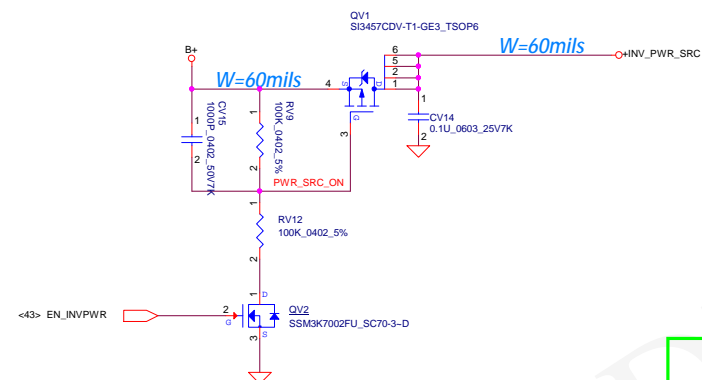
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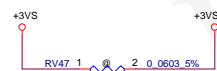
LCD power control



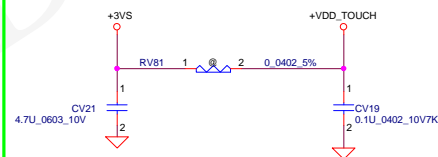
LCD backlight power control



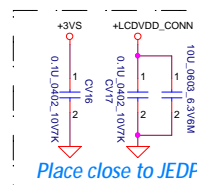
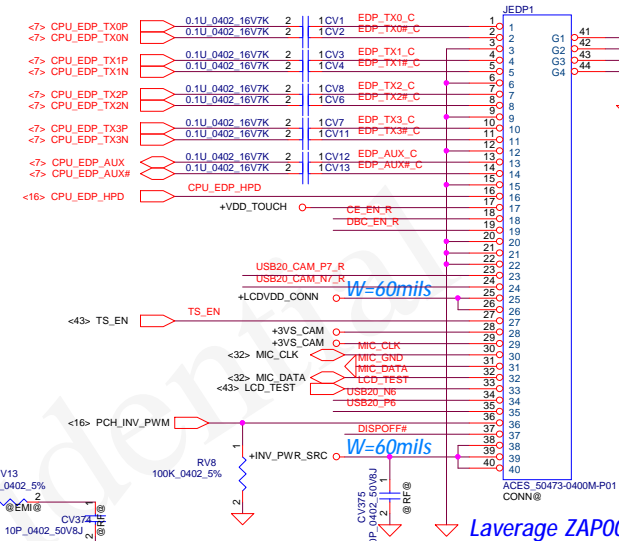
Webcam power control



Touch screen panel power control



eDP connector

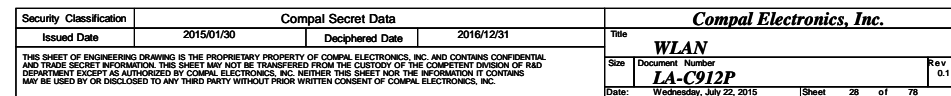


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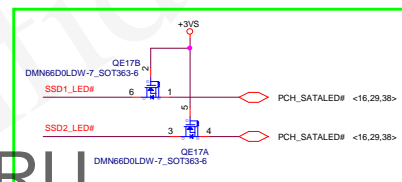
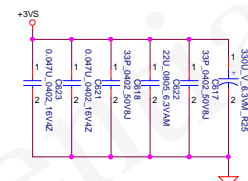
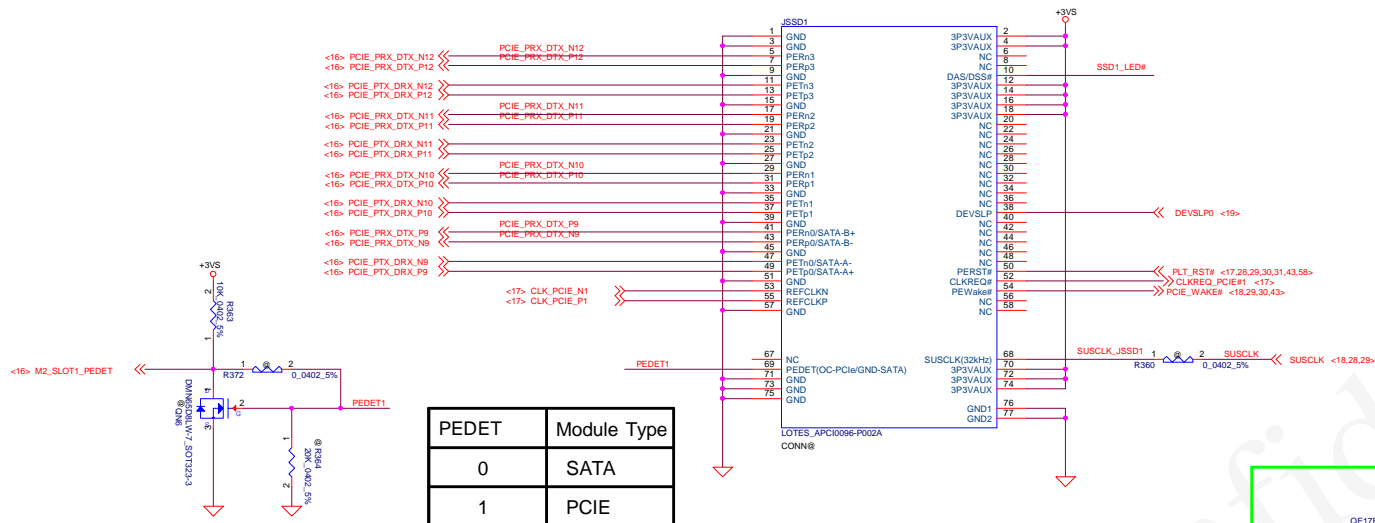
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				Custom	LA-C912P
				Date:	Wednesday, July 22, 2015
				Sheet	25 of 78

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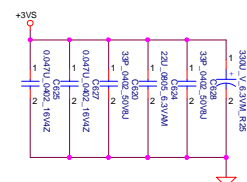
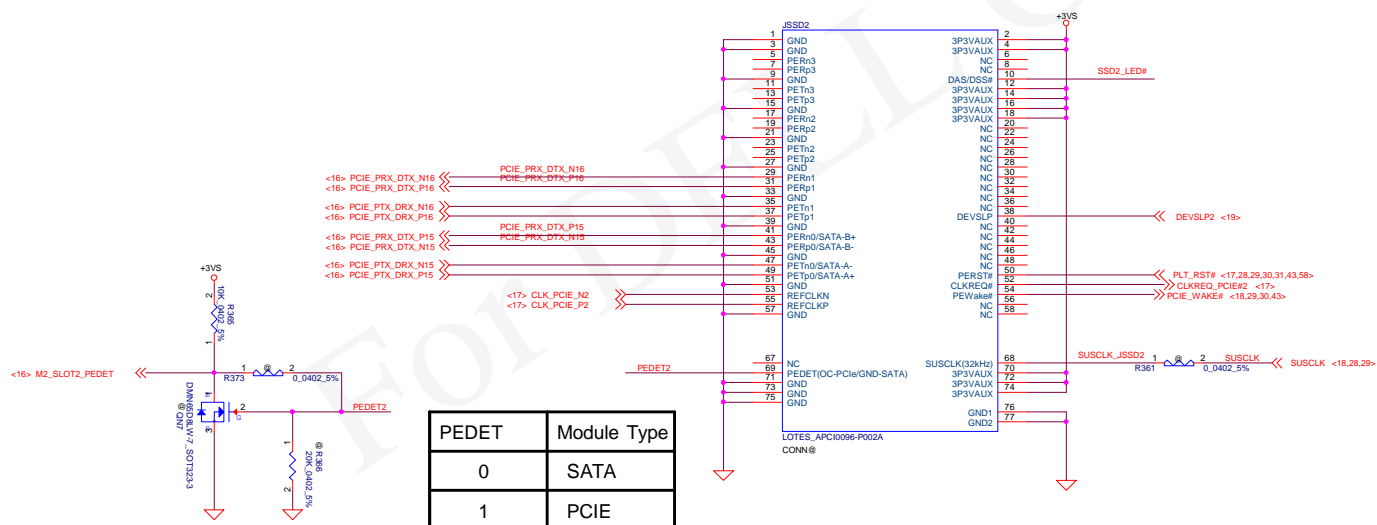
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Issued Date		2015/01/30	Deciphered Date		2016/12/31			
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						Size	Document Number	Rev
						Custom	LA-C912P	0.1
						Date:	Wednesday, July 22, 2015	Sheet 26 of 78



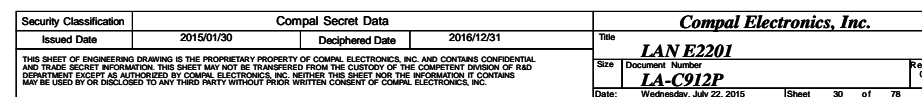
SSD NGFF slot_1 Key M

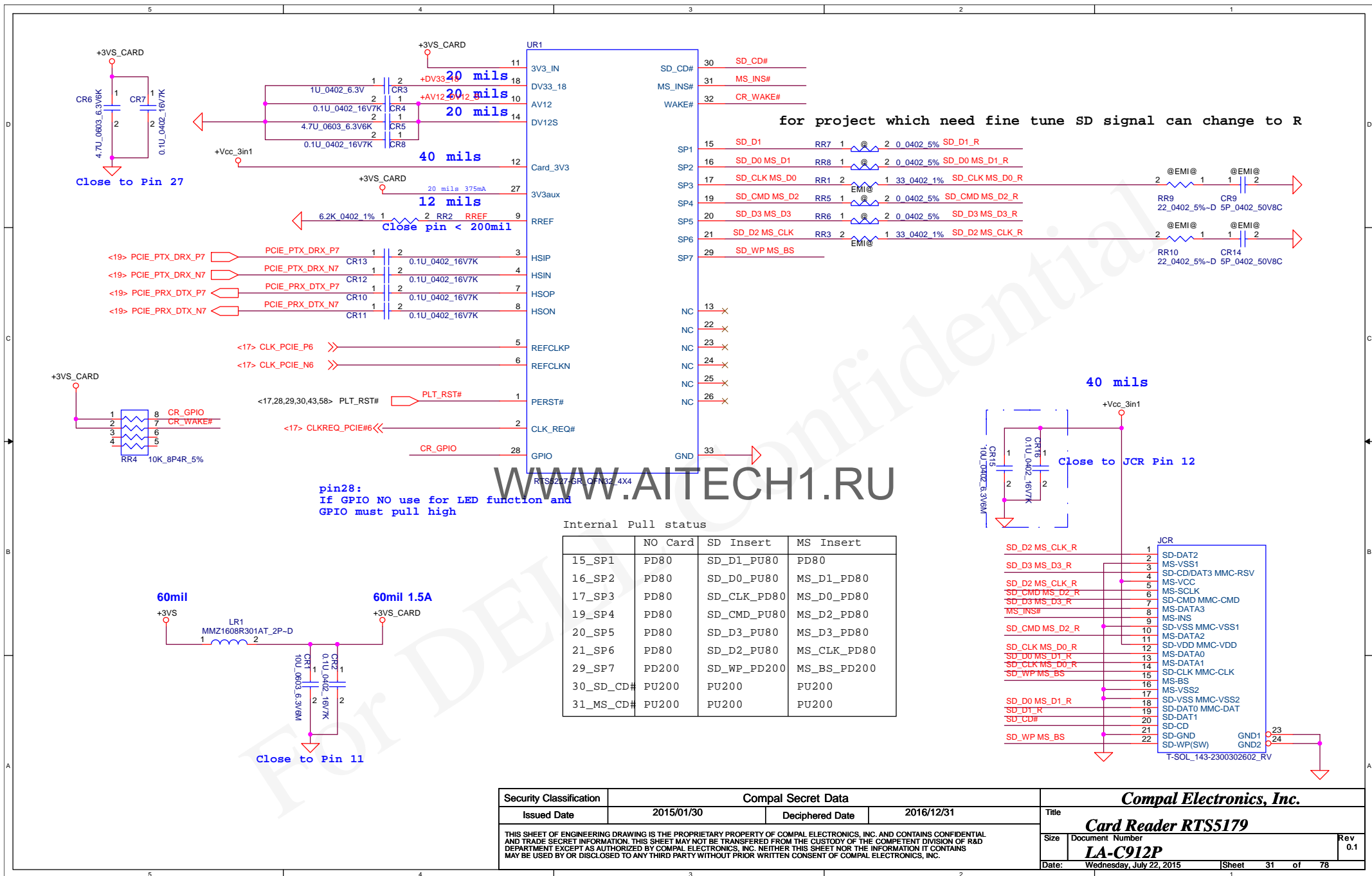


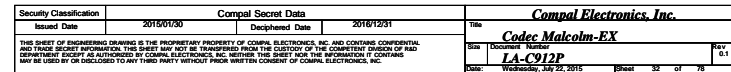
SSD NGFF Slot_2 Key M



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					LA-C912P
				Date	Wednesday, July 22, 2015
				Sheet	29 of 78
				Rev	0.1

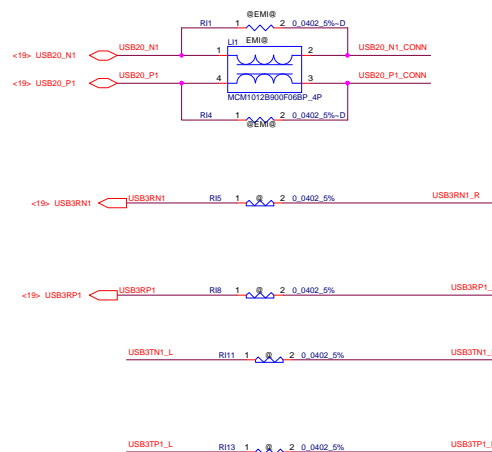
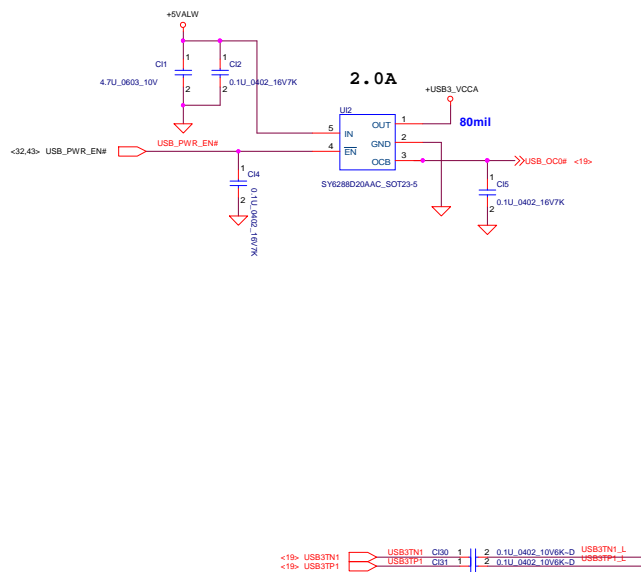






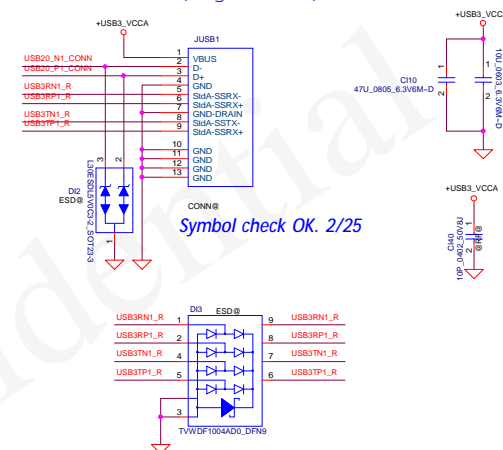
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Issued Date	2015/01/30	Deciphered Date	2016/12/31	Title Reserved Page	
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				IA-C912P	
Date: Wednesday, July 22, 2015				Sheet	33 of 78
				Rev	0.1



JUSB1

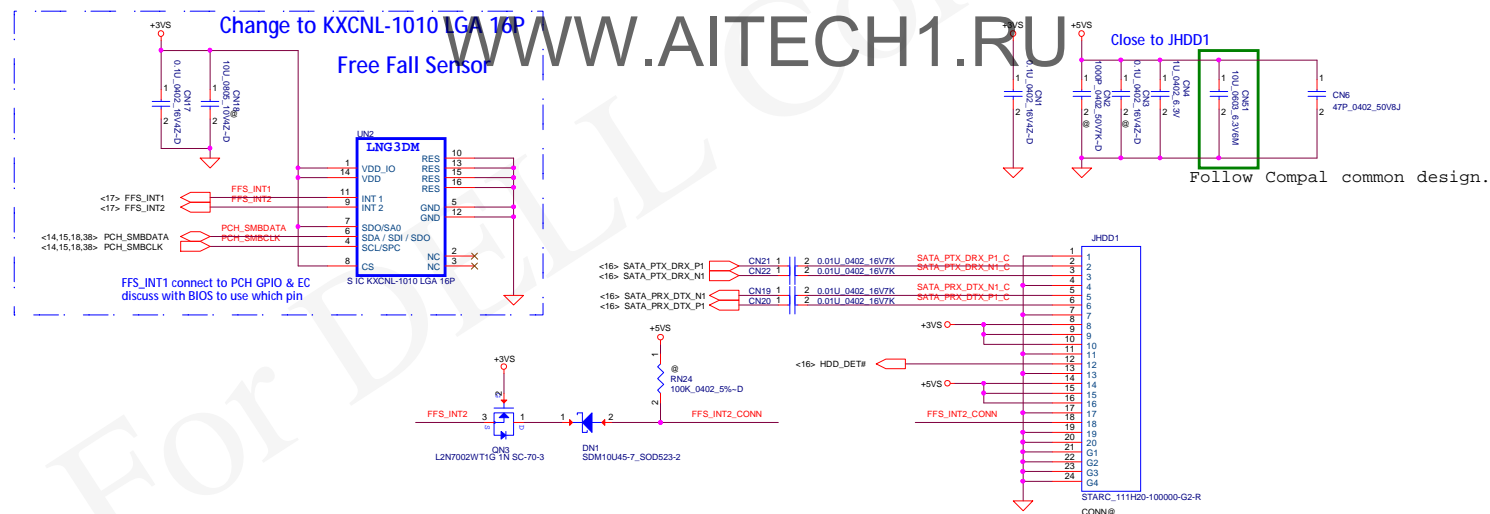
On MB (Right Side)



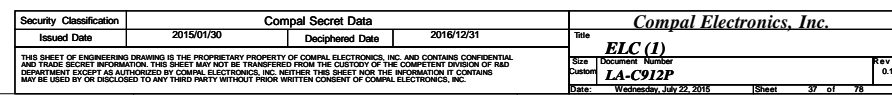
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JUSB2 change to TypeC

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				Date	Wednesday, July 22, 2015
				Sheet	34 of 76



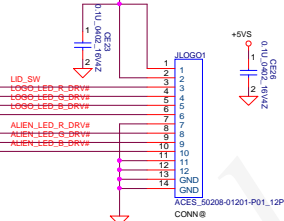
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Issued Date	2015/01/30	Deciphered Date	2016/12/31	Title	
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				Size	DocuSign Number
				LA-C912P	
Date:	Wednesday, July 22, 2015	Sheet	36	of	78



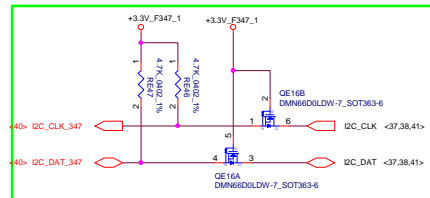
MAX7313 change to TI TLC59116F PWM expander

Power LED

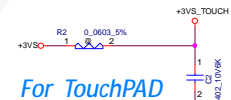
W=20mils



For IND/TP/HDD/PWR

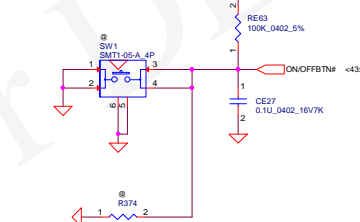


WWW.AITECH1.RU



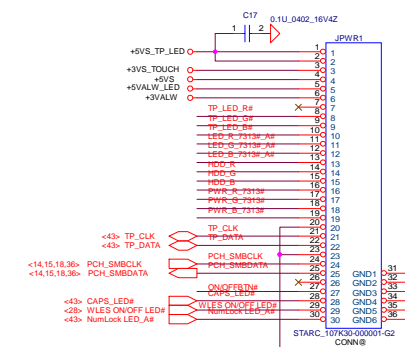
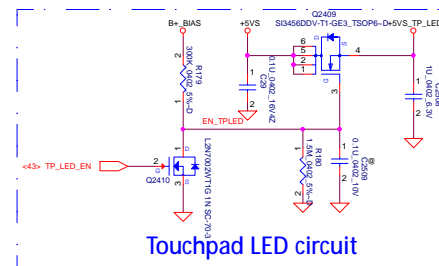
Power ON Circuit

ON/OFF switch



ON/OFF switch power button
Bottom Side pop only before MP

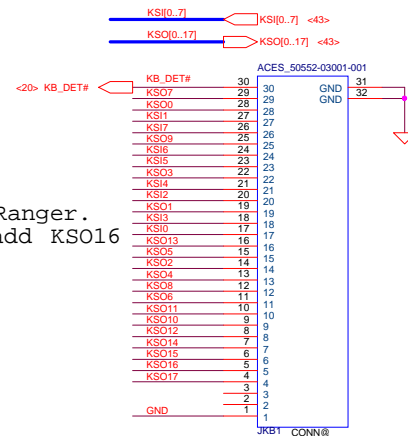
Touchpad LED circuit



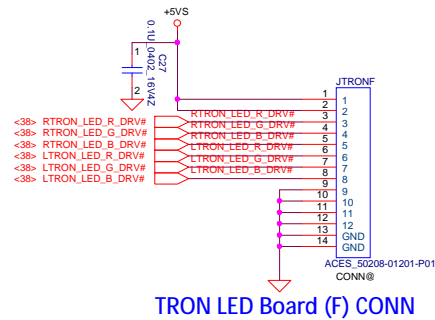
Change Symbol OK
2/18 -Tarry

Security Classification		Compal Secret Data		Title	
Issued Date	2015/01/30	Deciphered Date	2016/12/31	ELC (2)/TP/PWR SW	
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				Sheet	LA-C912P
				Date	Wednesday, July 22, 2015
				Sheet	38 of 76

INT_KBD Conn.



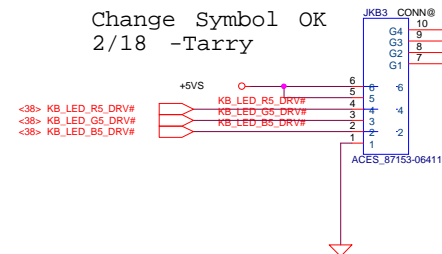
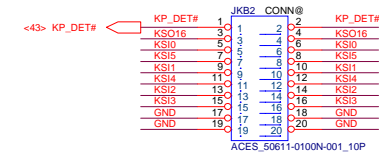
Net follow Ranger.
Only Pin26 add KSO16



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Hot Key Conn.
PWM

Change Symbol OK
2/18 -Tarry

Hot Key Conn.
Key Pad

Compal Electronics, Inc.			
Title			
KB/HotKey conn			
Size	Document	Number	Rev
		LA-C912P	0.1
Date:	Wednesday, July 22, 2015	Sheet	39 of 78

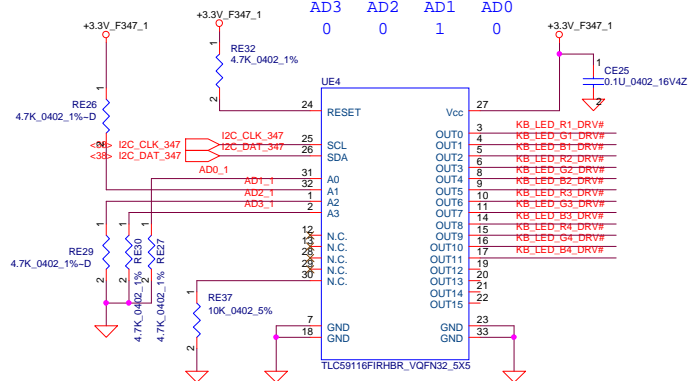
1/28 ADD

+5VS RE104 1 2 0.0603.5% +5V_LED
 +3VS RE105 1 2 0.0603.5%

K/B Backlight

AD3 AD2 AD1 AD0

0 0 1 0



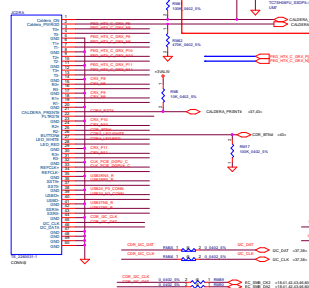
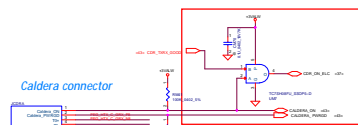
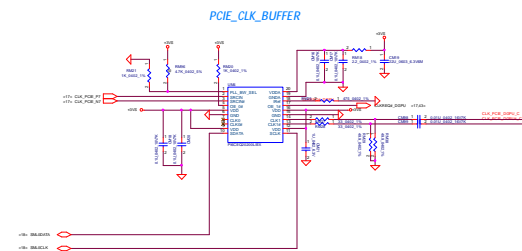
KB BL LED

WWW.ATECH1.RU

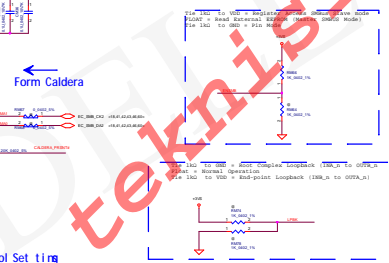
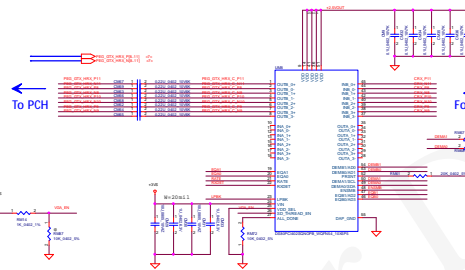
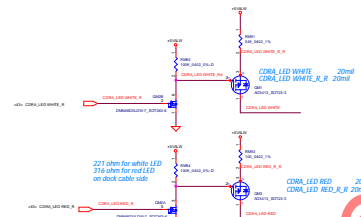
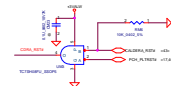


Compal Electronics, Inc.

Title			ELC(3)
Size	Document Number	Rev	
	LA-C912P	0.1	
Date:	Wednesday, July 22, 2015	Sheet	40 of 78



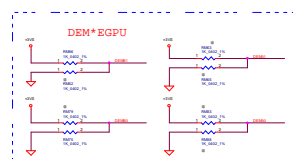
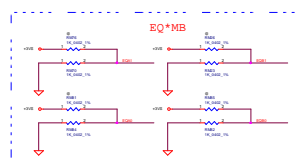
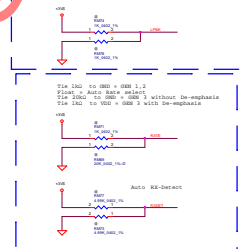
Follow ZAP00 design.

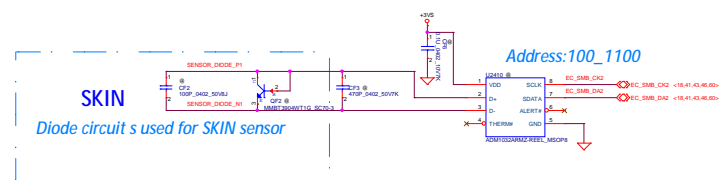


EQ Setting					
Line	EQ	dB	at 2.5G	at 10G	Suggested Use
1	Q	0	-1.5	-1.5	<2 inch trace
2	Q	0	-1.5	-1.5	5 inch <48 trace
3	Q	0	0	0	5 inch <48 trace
4	R	1	-1.5	-1.5	10 inch <48 trace
5	R	1	-1.5	-1.5	10 inch <48 trace
6	R	1	-1.5	-1.5	10 inch <48 trace
7	R	1	-1.5	-1.5	20 to 30 inch <48 trace
8	R	1	-1.5	-1.5	30 inch <48 trace
9	R	1	-1.5	-1.5	30 inch <48 trace
10	R	1	-1.5	-1.5	30 inch <48 trace
11	R	1	-1.5	-1.5	10m, 50m cable
12	R	1	-1.5	-1.5	
13	L	0	-25.0	-25.0	
14	L	1	-23.0	-23.0	10m - 12 cables
15	L	1	-23.0	-23.0	

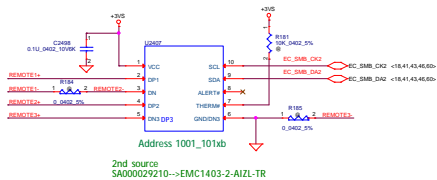
level	DEMA DEM1	DEMA DEM2	DEMA diff	Suggested Use
1	0	0	0	<5 inch 4" - 8" trace
2	0	R	0	<5 inch 4" - 8" trace
3	0	F	-3.5	<5 inch 4" - 8" trace
4	0	L	0	<5 inch 4" - 8" trace
5	R	0	-4.5	<5 inch 4" - 8" trace
6	R	R	-6	<5 inch 4" - 8" trace
7	R	F	0	<5 inch 4" - 8" trace
8	R	L	-3.5	<5 inch 4" - 8" trace
9	F	0	-6	<5 inch 4" - 8" trace
10	F	R	0	<5 inch 4" - 8" trace
11	F	F	-3.5	<5 inch 4" - 8" trace
12	F	L	-6	<5 inch 4" - 8" trace
13	L	0	0	<5 inch 4" - 8" trace
14	L	R	-3.5	<5 inch 4" - 8" trace
15	L	F	-6	<5 inch 4" - 8" trace
16	L	L	-9	<20 inch 4" - 8" trace

Level	Pin Set ting	Description
1	0	1000 4- 4 trace
2	255	1000 4- 4 trace
3	255	1000 4- 4 trace
4	1	1000 4- 4 trace

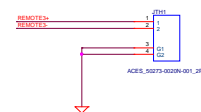




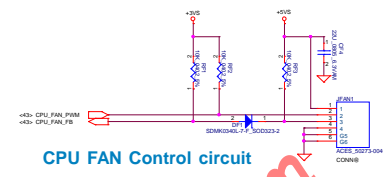
Fintek thermal sensor-> CPU core, DIMM



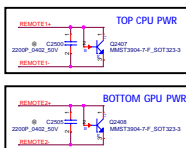
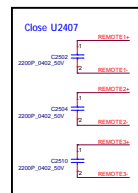
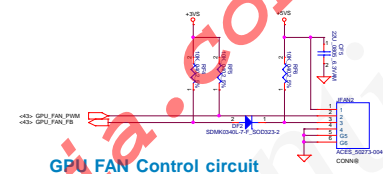
Thermal Board for SSD



CPU FAN Control circuit

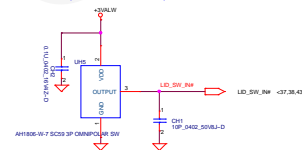


GPU FAN Control circuit

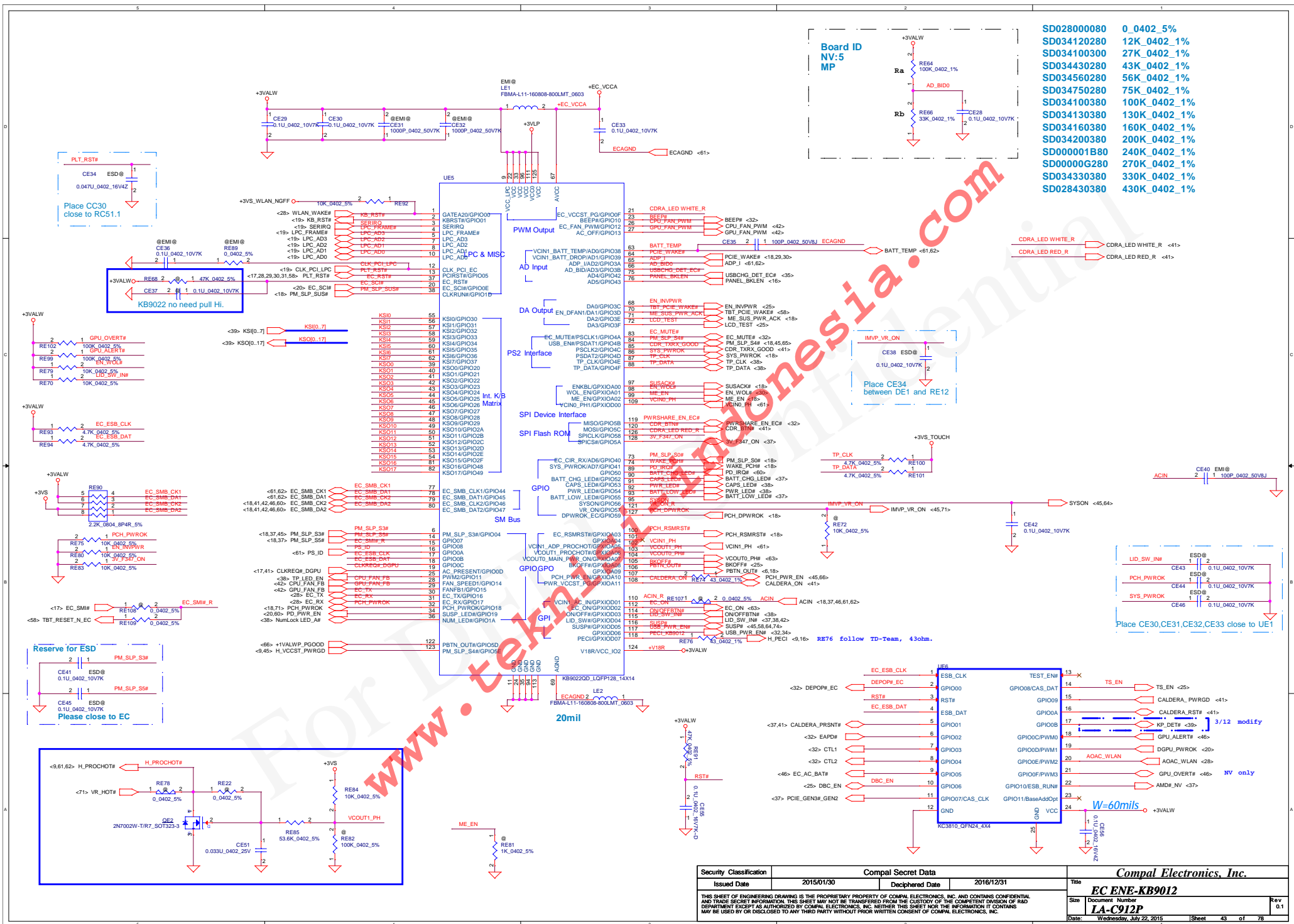


REMOTE1,2 (+/-):
Trace width/space:10/10 mil
Trace length:-8"

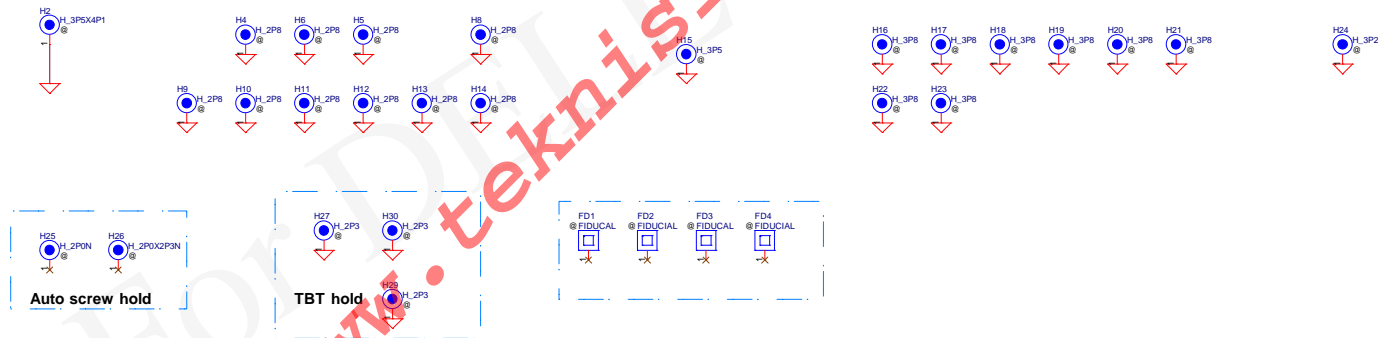
Lid Switch (Hall Effect Switch)



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File	FAN/TP/PWR SW	Rev
Size	1A-C912P	Rev
Date	Wednesday, July 21, 2015	Sheet 24 of 28

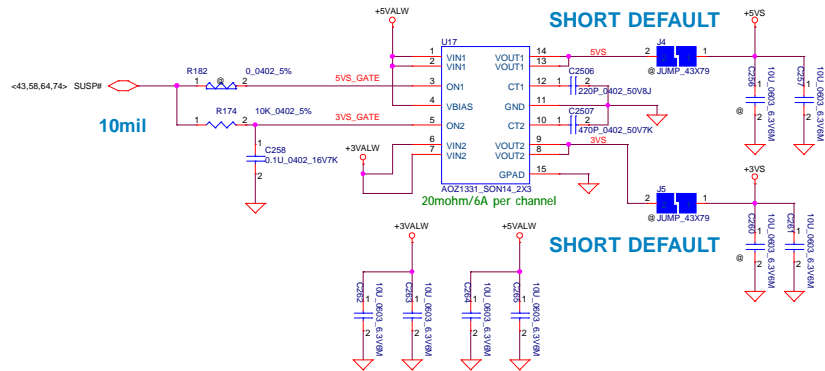


Screw Hole

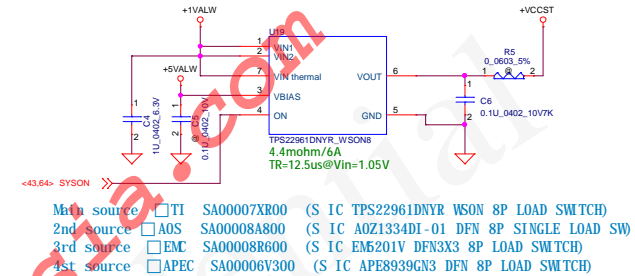


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				Document Number
				LA-C912P
				Rev
				0.1
				Date
				Wednesday, July 22, 2015
				Sheet
				44 of 78

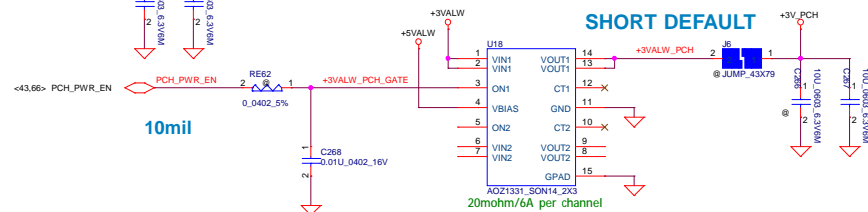
+5VS and +3VS switch



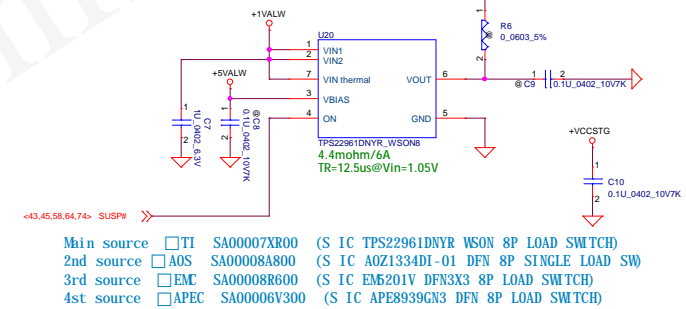
+VCCST Load Switch



+3VALW_PCH switch



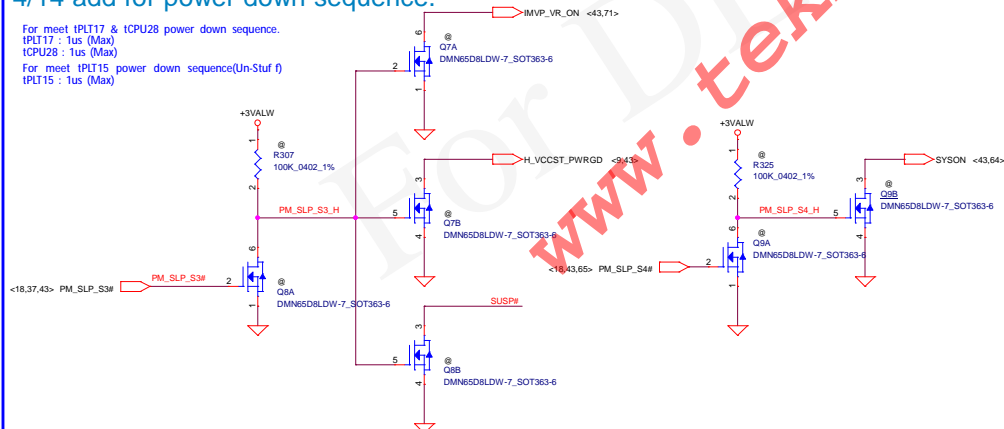
+VCCSTG source



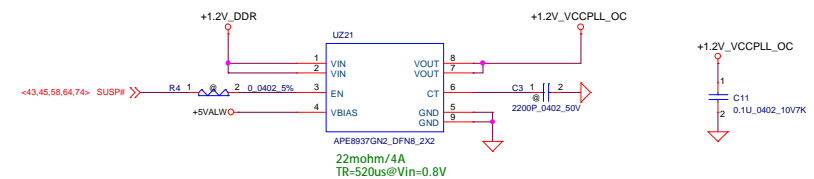
4/14 add for power down sequence.

For meet tPLT17 & tCPU28 power down sequence.
 tPLT17 : 1us (Max)
 tCPU28 : 1us (Max)

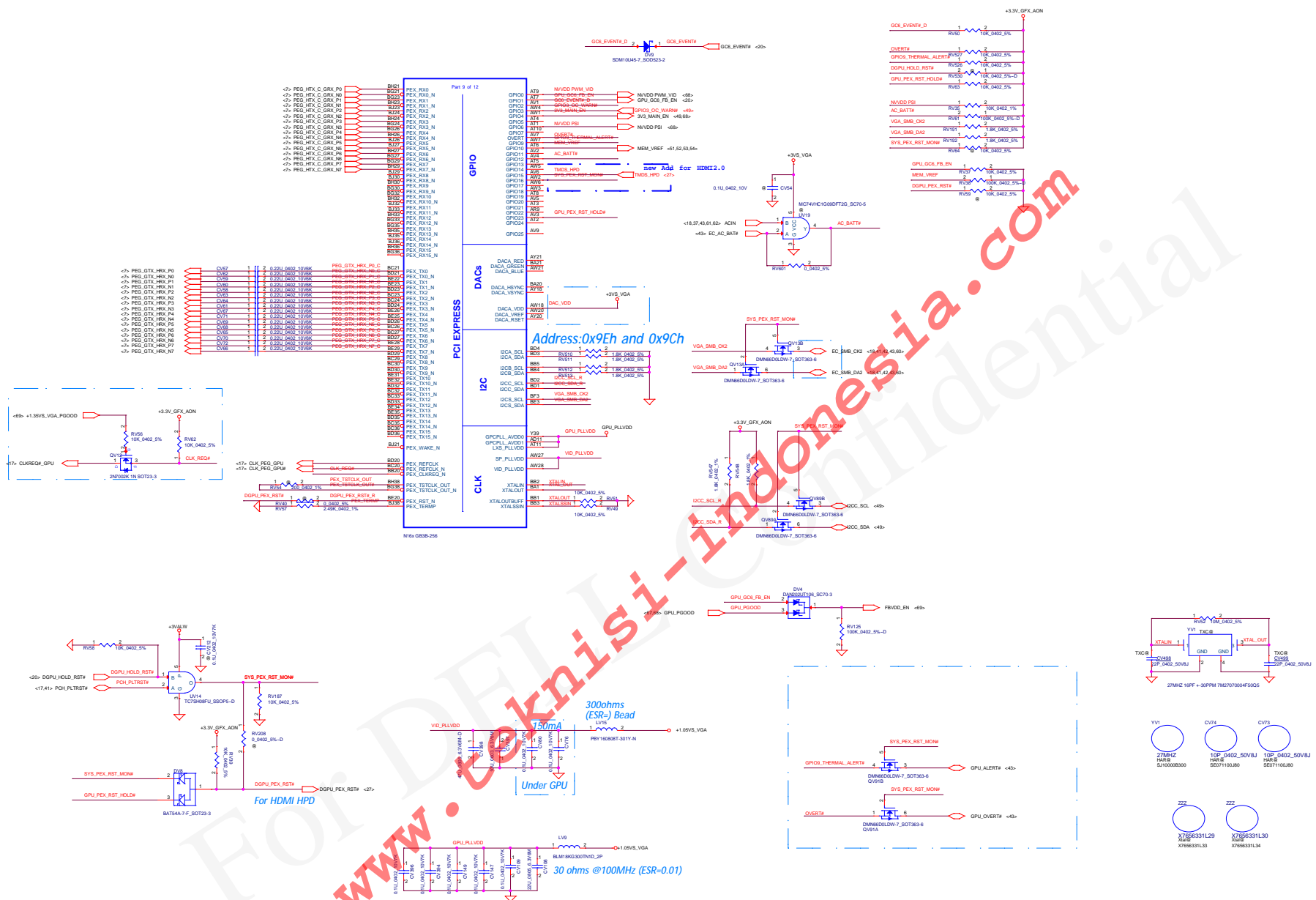
For meet tPLT15 power down sequence(Un-Stuf f)
 tPLT15 : 1us (Max)



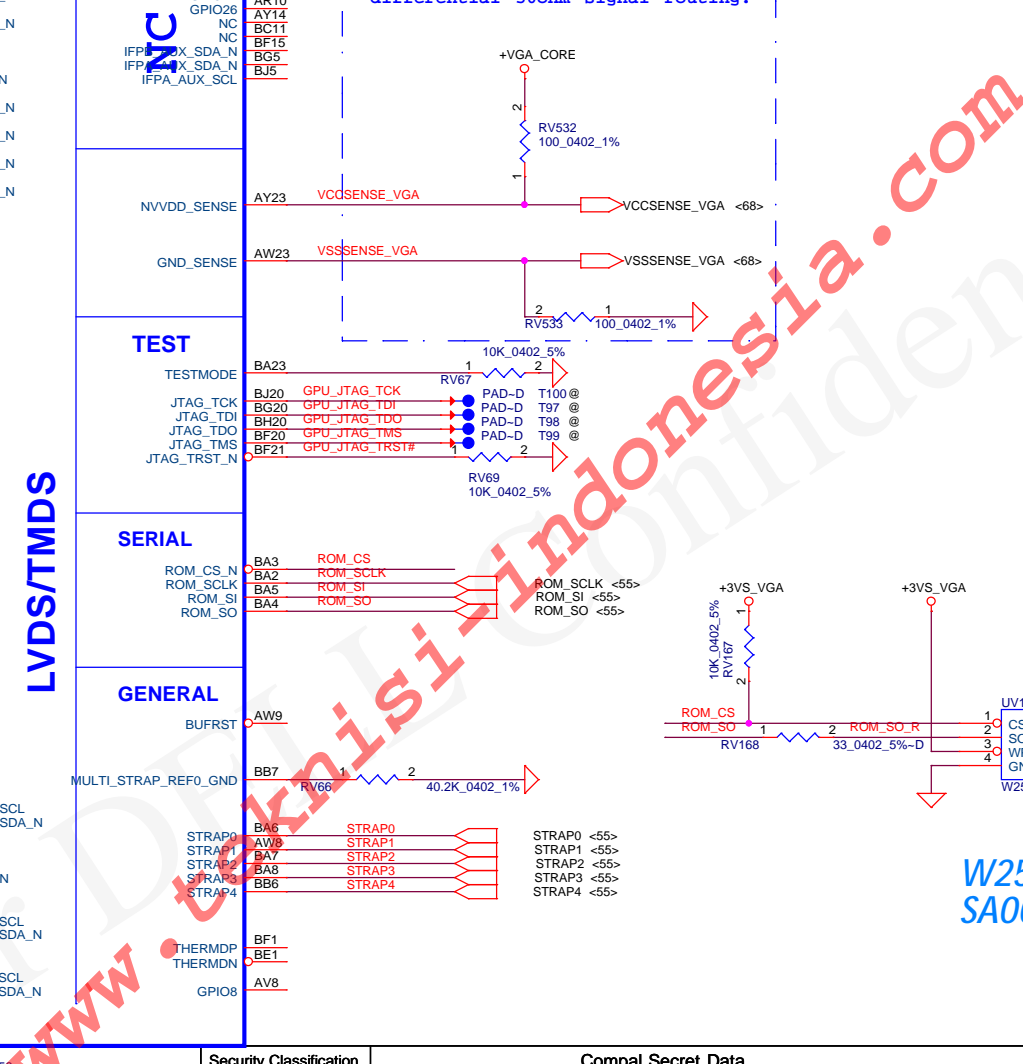
+1.2V_VCCPLL_OC



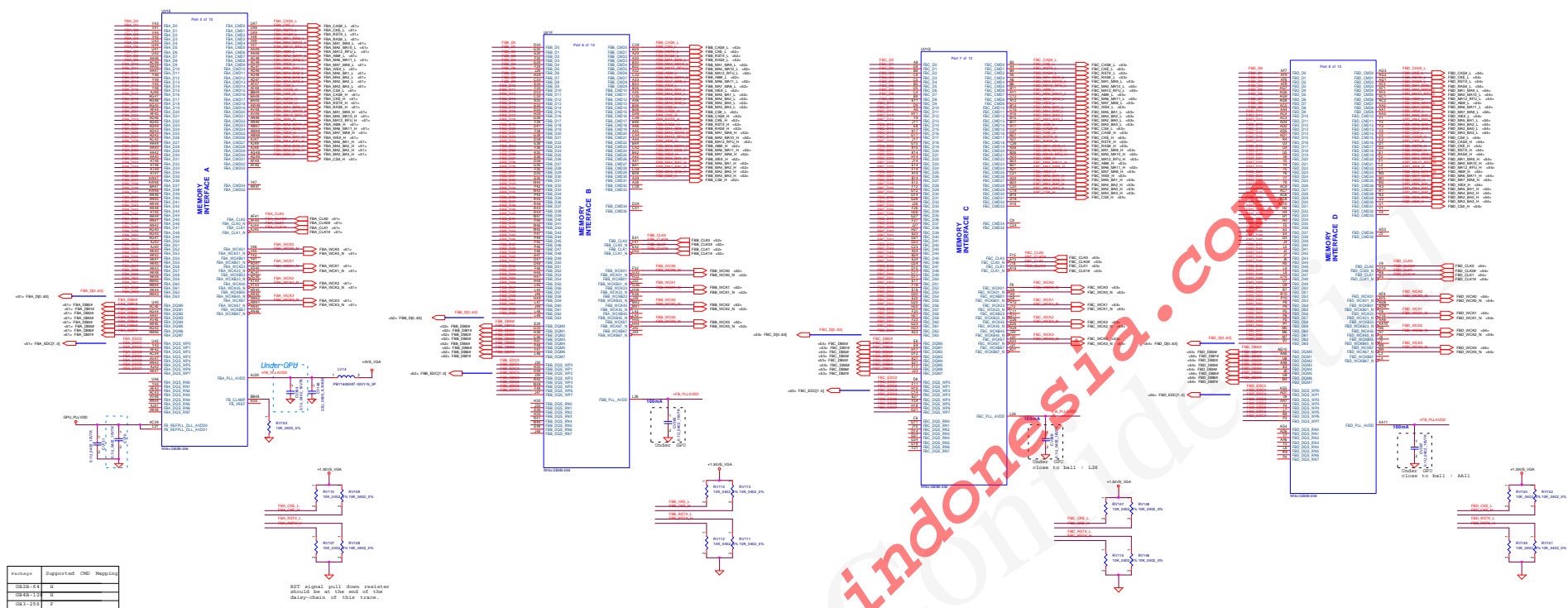
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2015/01/30	Deciphered Date	2016/12/31	Title	DC/DC Interface
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				Rev	0.1
				Date	Wednesday, July 22, 2015
				Sheet	45 of 78



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Rev	1.00	Rev	1.00
LA-C912P			
Rev	1.00	Rev	1.00
Rev	1.00	Rev	1.00

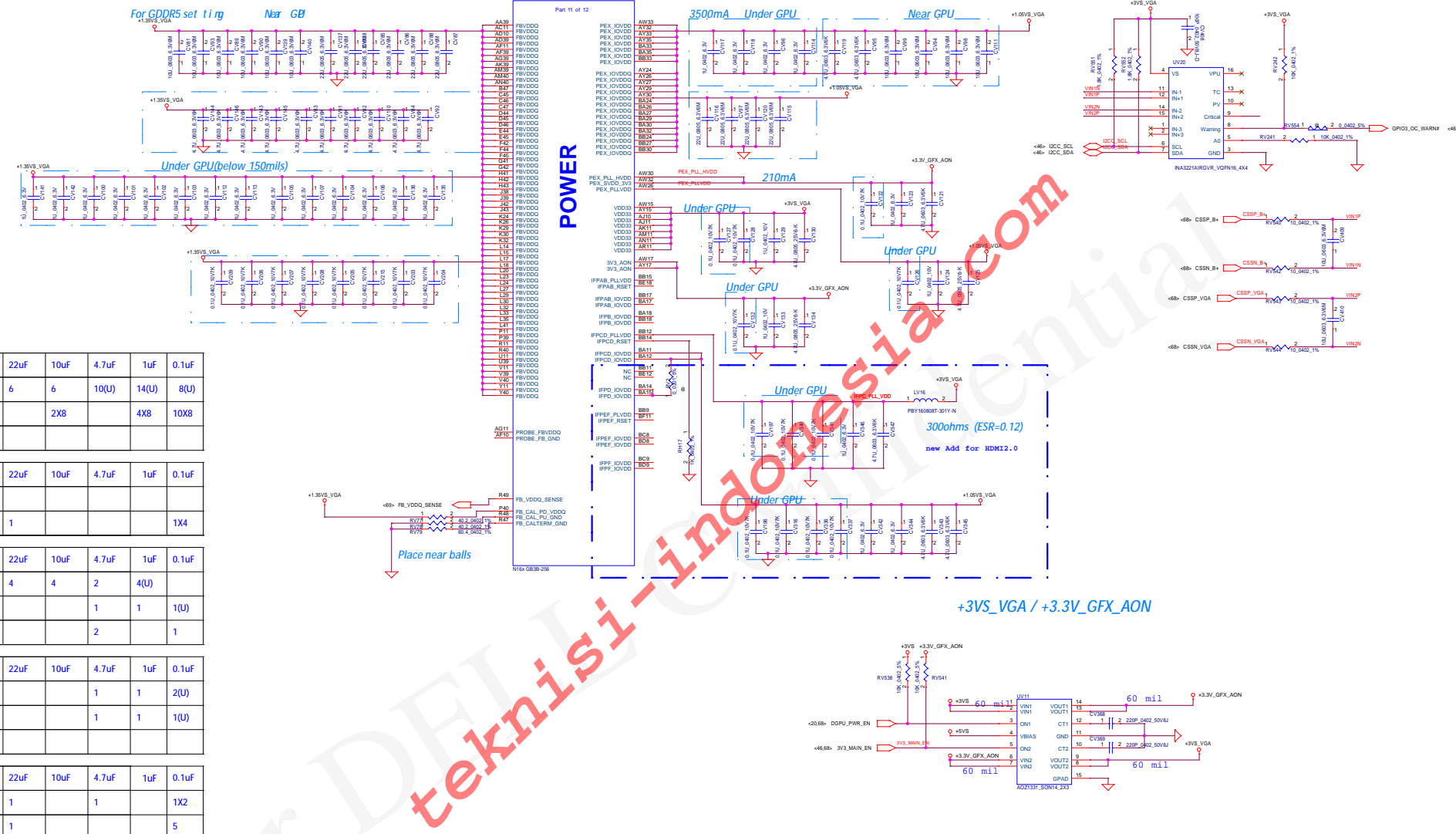


Title		<i>N15P-GX (1/5) PEG & DAC</i>	
Size B	Document Number <i>LA-C912P</i>	Rev 0.1	
Date:	Wednesday, July 22, 2015	Sheet	47 of 78



Package	Supported QMD Mapping
QMD30-64	M
QMD30-128	M
QMD30-256	F

Node #	Address	Node #	Address	Node #	Address
QMD0	0x0000	QMD1	0x0001	QMD2	0x0002
QMD3	0x0003	QMD4	0x0004	QMD5	0x0005
QMD6	0x0006	QMD7	0x0007	QMD8	0x0008
QMD9	0x0009	QMD10	0x000A	QMD11	0x000B
QMD12	0x000C	QMD13	0x000D	QMD14	0x000E
QMD15	0x000F	QMD16	0x0010	QMD17	0x0011
QMD18	0x0012	QMD19	0x0013	QMD20	0x0014
QMD21	0x0015	QMD22	0x0016	QMD23	0x0017
QMD24	0x0018	QMD25	0x0019	QMD26	0x001A
QMD27	0x001B	QMD28	0x001C	QMD29	0x001D
QMD30	0x001E	QMD31	0x001F	QMD32	0x0020
QMD33	0x0021	QMD34	0x0022	QMD35	0x0023
QMD36	0x0024	QMD37	0x0025	QMD38	0x0026
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QMD45	0x002D	QMD46	0x002E	QMD47	0x002F
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QMD51	0x0033	QMD52	0x0034	QMD53	0x0035
QMD54	0x0036	QMD55	0x0037	QMD56	0x0038
QMD57	0x0039	QMD58	0x003A	QMD59	0x003B
QMD60	0x003C	QMD61	0x003D	QMD62	0x003E
QMD63	0x003F	QMD64	0x0040	QMD65	0x0041
QMD66	0x0042	QMD67	0x0043	QMD68	0x0044
QMD69	0x0045	QMD70	0x0046	QMD71	0x0047
QMD72	0x0048	QMD73	0x0049	QMD74	0x004A
QMD75	0x004B	QMD76	0x004C	QMD77	0x004D
QMD78	0x004E	QMD79	0x004F	QMD80	0x0050
QMD81	0x0051	QMD82	0x0052	QMD83	0x0053
QMD84	0x0054	QMD85	0x0055	QMD86	0x0056
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QMD90	0x005A	QMD91	0x005B	QMD92	0x005C
QMD93	0x005D	QMD94	0x005E	QMD95	0x005F
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QMD108	0x006C	QMD109	0x006D	QMD110	0x006E
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QMD150	0x0096	QMD151	0x0097	QMD152	0x0098
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QMD252	0x00FC	QMD253	0x00FD	QMD254	0x00FE
QMD255	0x00FF	QMD256	0x0100	QMD257	0x0101
QMD258	0x0102	QMD259	0x0103	QMD260	0x0104
QMD261	0x0105	QMD262	0x0106	QMD263	0x0107
QMD264	0x0108	QMD265	0x0109	QMD266	0x010A
QMD267	0x010B	QMD268	0x010C	QMD269	0x010D
QMD270	0x010E	QMD271	0x010F	QMD272	0x0110
QMD273	0x0111	QMD274	0x0112	QMD275	0x0113
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QMD342	0x0156	QMD343	0x0157	QMD344	0x0158
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QMD375	0x0177	QMD376	0x0178	QMD377	0x0179
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QMD390	0x0186	QMD391	0x0187	QMD392	0x0188
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QMD396	0x018C	QMD397	0x018D	QMD398	0x018E
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QMD402	0x0192	QMD403	0x0193	QMD404	0x0194
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QMD510	0x01FE	QMD511	0x01FF	QMD512	0x0200
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QMD522	0x020A	QMD523	0x020B	QMD524	0x020C
QMD525	0x020D	QMD526	0x020E	QMD527	0x020F
QMD528	0x0210	QMD529	0x0211	QMD530	0x0212
QMD531	0x0213	QMD532	0x0214	QMD533	0x0215
QMD534	0x0216	QMD535	0x0217	QMD536	0x0218
QMD537	0x0219	QMD538	0x021A	QMD539	0x021B
QMD540	0x021C	QMD541	0x021D	QMD542	0x021E
QMD543	0x021F	QMD544	0x0220	QMD545	0x0221
QMD546	0x0222	QMD547	0x0223	QMD548	0x0224
QMD549	0x0225	QMD550	0x0226	QMD551	0x0227
QMD552	0x0228	QMD553	0x0229	QMD554	0x022A
QMD555	0x022B	QMD556	0x022C	QMD557	0x022D
QMD558	0x022E	QMD559	0x022F	QMD560	0x0



FBVDD/FBVDDQ (+1.35VS_VGA)	22uF	10uF	4.7uF	1uF	0.1uF
GPU	6	6	10(U)	14(U)	8(U)
Memory		2X8		4X8	10X8

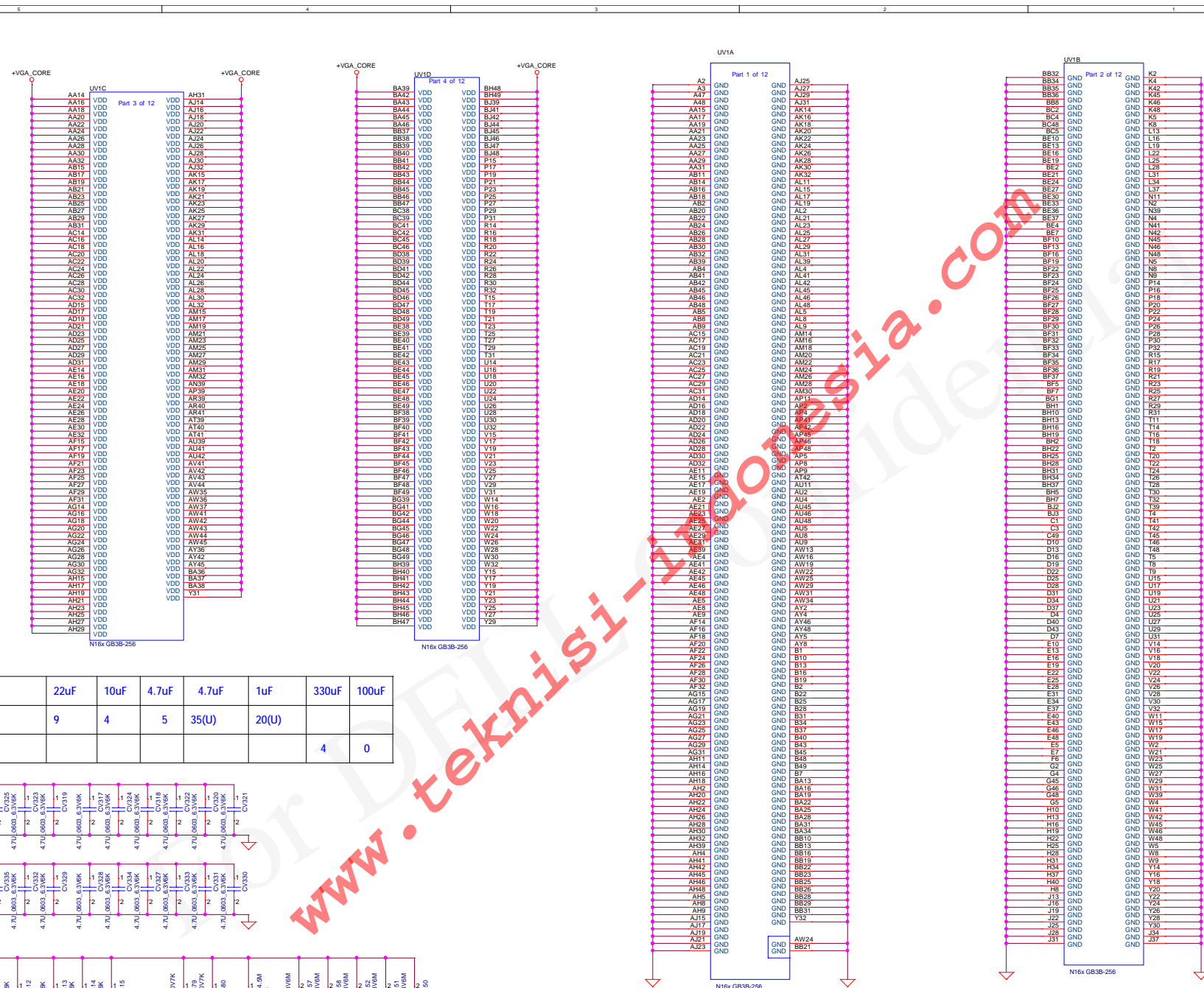
	22uF	10uF	4.7uF	1uF	0.1uF
FbX_PLL_DLL_AVDD +GPU_PLIVDD(1.05)					
FbX_PLL_AVDD +FB_PLLAVDD(3.3)	1				1X4

	22uF	10uF	4.7uF	1uF	0.1uF
PEX_I0VDD/Q(1.05)	4	4	2	4(U)	
PEX_PL1VDD(1.05)			1	1	1(U)
PEX_SVDD_3V3 +3.3V_GFX_A0N			2		1

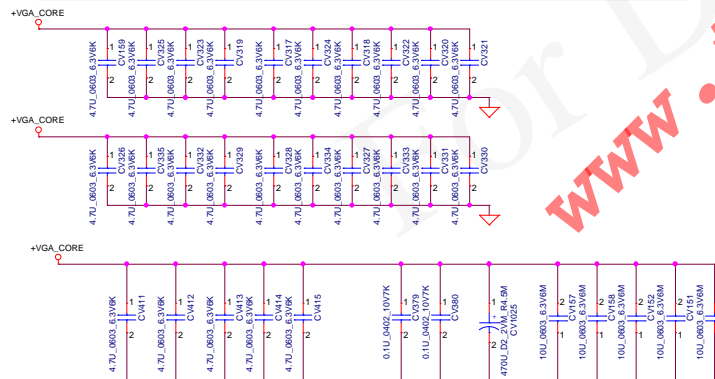
	22uF	10uF	4.7uF	1uF	0.1uF
3V3_Main +3V5_VGA			1	1	2(U)
3V3_AON +3.3V_GFX_AON			1	1	1(U)

1.05V	22uF	10uF	4.7uF	1uF	0.1uF
SP_PLLVDD VID_PLLVDD	1		1		1X2
GPU_PLIAVDD	1				5

Security Classification	Compul Secret Data			Title
Issued Date	2015/01/30	Deciphered Date	2016/12/31	<i>NISP-GX (1/5) PEG & DAC</i>
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				LA-C912P 1/1/2015 49 of 78



NVVDD	22uF	10uF	4.7uF	4.7uF	1uF	330uF	100uF
+VGA_CORE	9	4	5	35(U)	20(U)		
						4	0

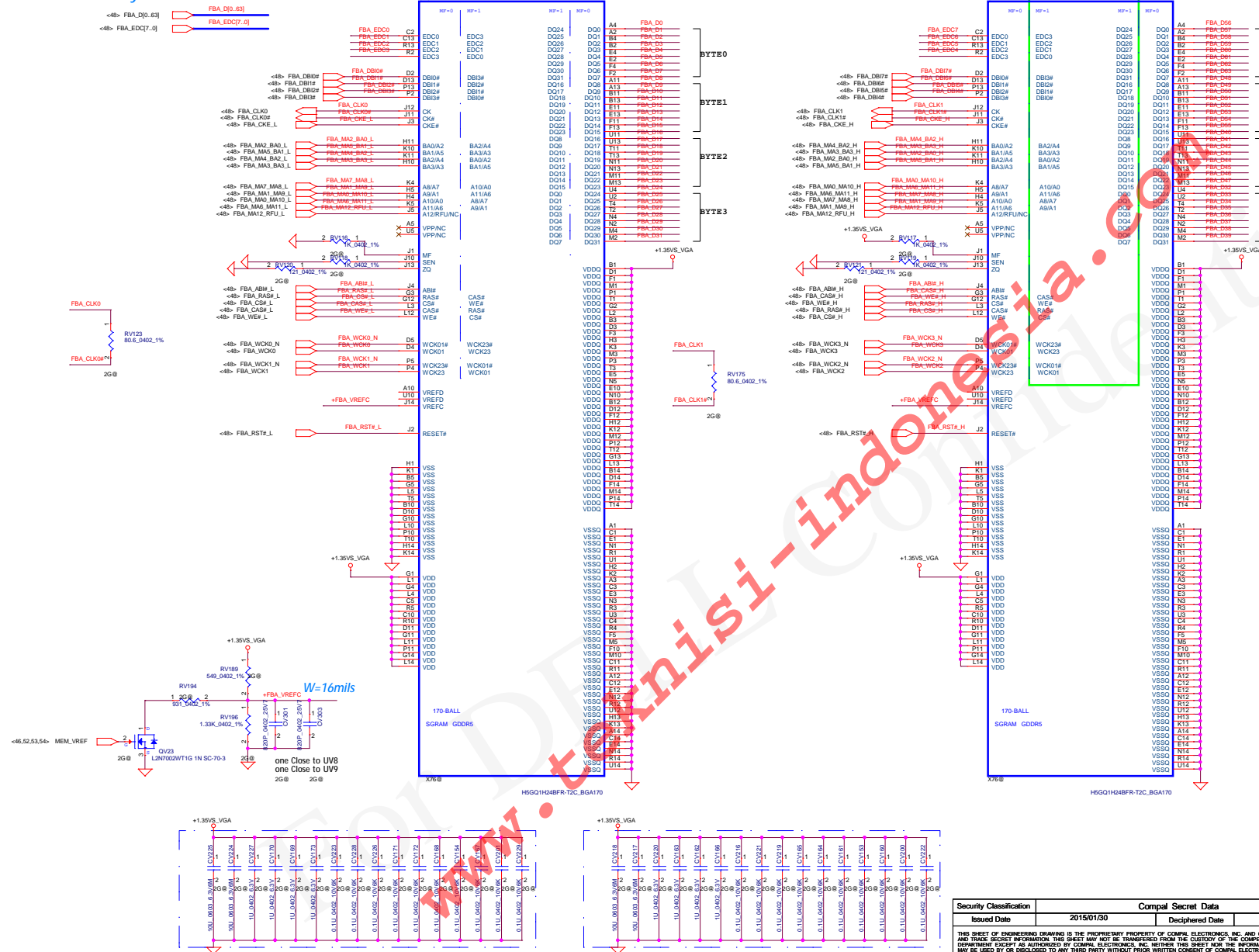


Security Classification	Compel Secret Data			Title
Issued Date	2015/01/30	Deciphered Date	2016/12/31	<i>NISP-GX (1/5) PEG & DAC</i>
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Date:	<i>Wednesday, July 22, 2015</i>	Sheet	50 of 78	Rev 0

Memory Partition A- L over 32 bits

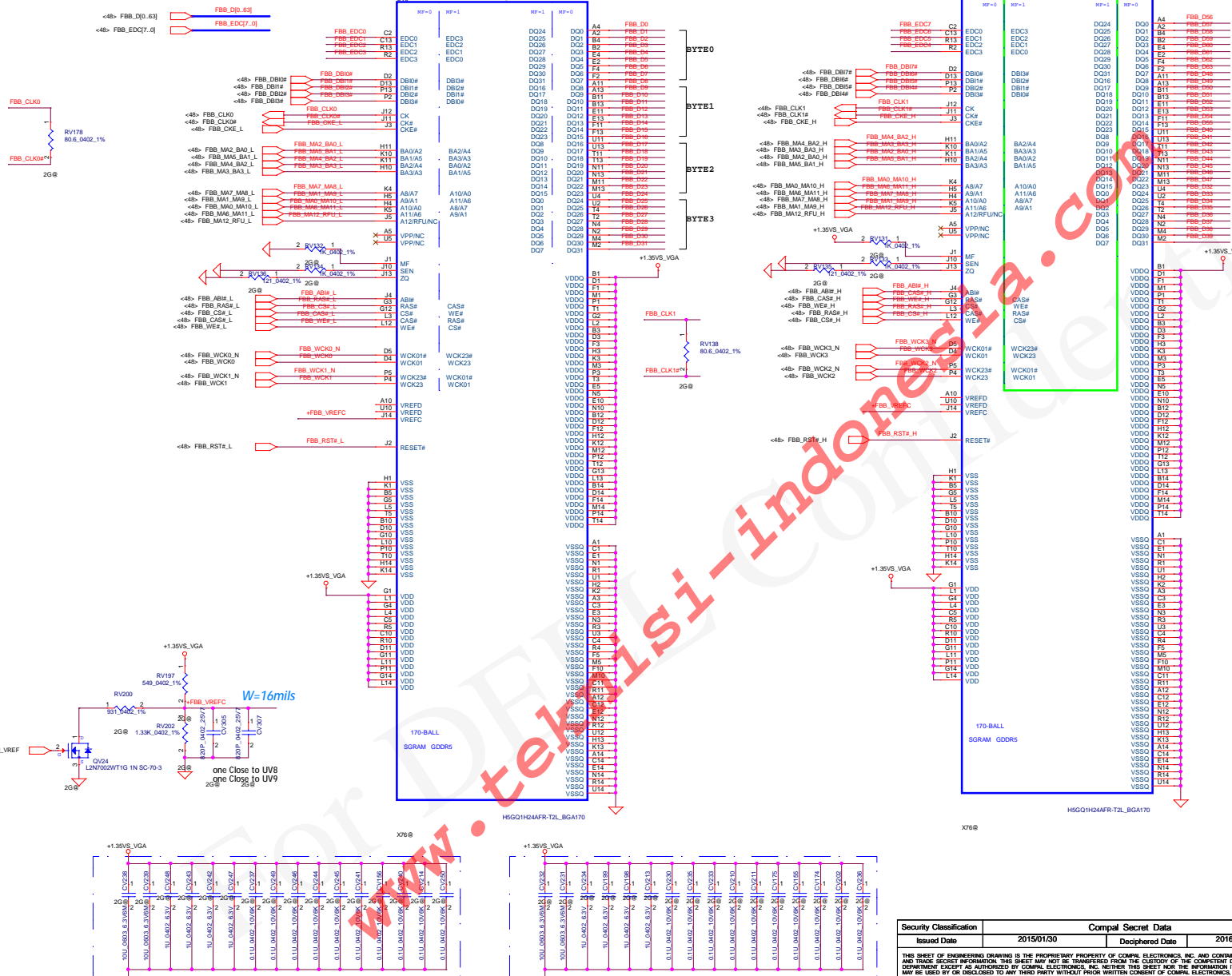
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MF=1



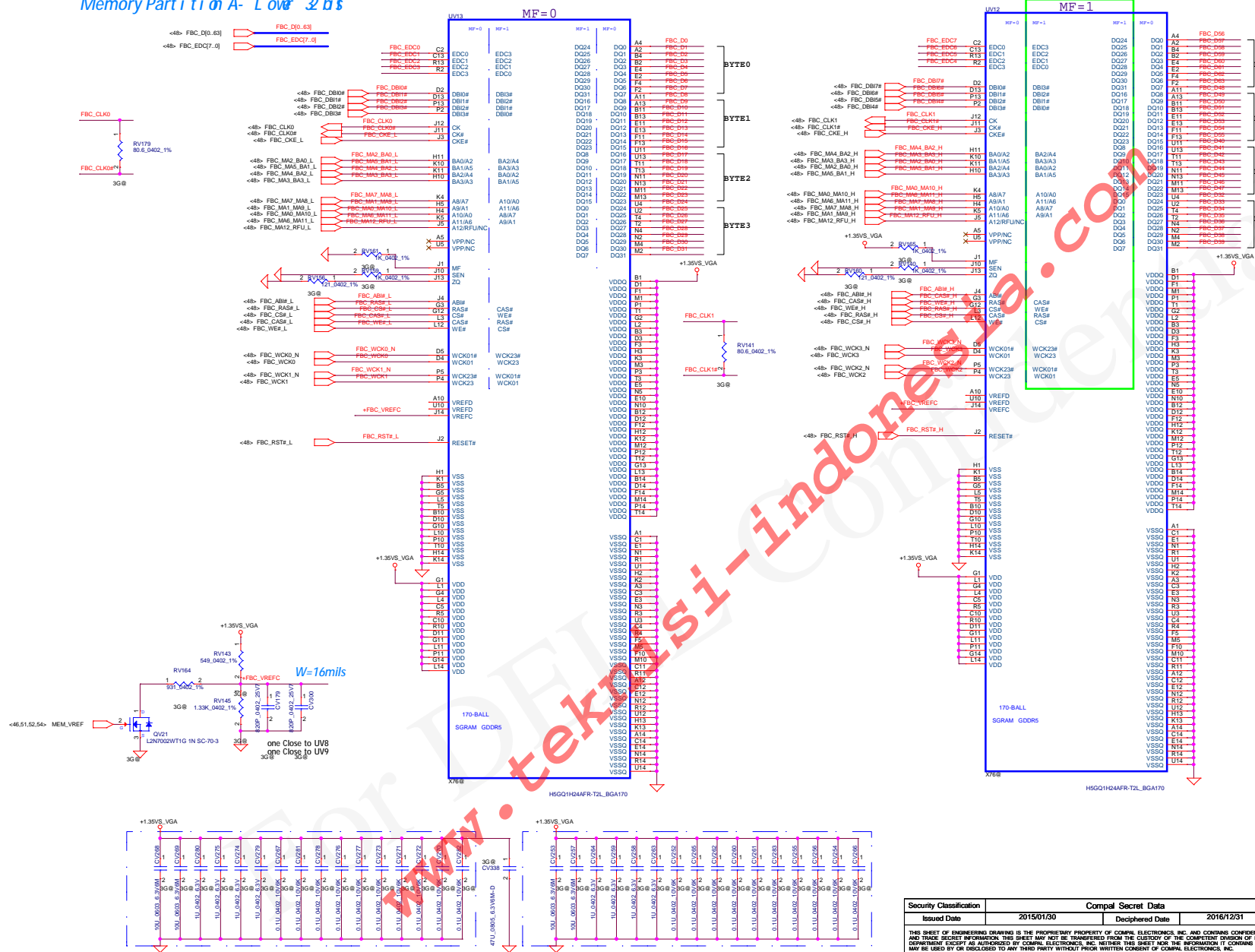
Security Classification	Compal Secret Data			Compal Electronics, Inc. N15P GDDR5 A Lower	
Issued Date	2015/01/30	Deciphered Date	2016/12/31	Title	
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					LA-C912P
				Date	Wednesday, July 22, 2015
				Sheet	01 of 78

Memory Partition A- Lower 32 bits

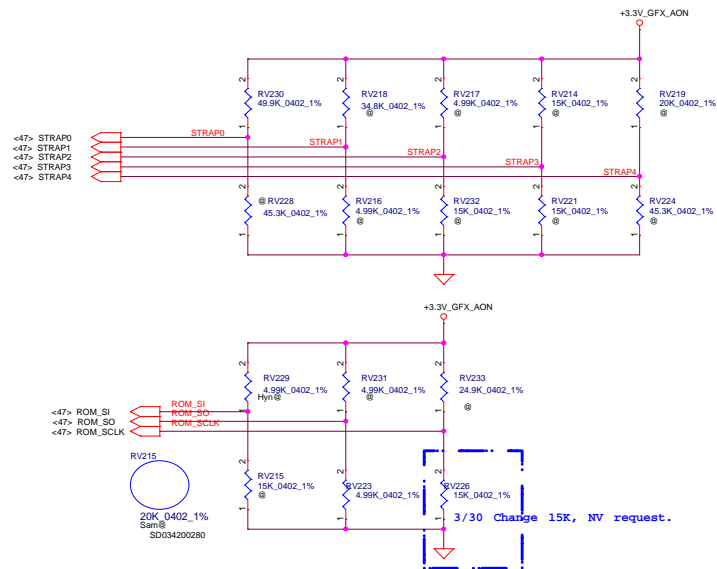


Security Classification	Compul Secret Data		<i>Compul Electronics, Inc.</i> <i>N15P GDDR5 A Upper</i>	
Issued Date	2015/01/30	Deciphered Date	2016/12/31	Title <i>N15P GDDR5 A Upper</i> <i>LA-C12P</i>
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			Date:	Wednesday, July 22, 2015 13:58 02 of 78

Memory Partition A- L over 32 bits



Security Classification	Compul Secret Data		Title		Compul Electronics, Inc.	
Issued Date	2015/01/30	Deciphered Date	2016/12/31	NISP GDDR5 A Upper		
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Date:	Wednesday, July 22, 2015		Sheet	53	of	78



R_pu

VRAM	Strap	ROM-SI
Hynix H5GC4H24MFR-T2C	0x2	PL 15K
Samsung K4G41325FC-HC03	0x3	PL 20K
Hynix H5GC4H24AJR-R0C	0x8	PH 5K

Set as Hynix H5GC4H24AJR-T2C @5G

	PU to 3V3	PD to GND
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111



PCI_DEVICE

SUB_VENDER

0- w/o dGPU ROM

1-w/ dGPU ROM

FB[1:0]

0-Reserved

1-Reserved

2-256M

3-Reserved

VGA_DEVICE

0- Non-permy 3D

1-

SMB_ALT_ADDR

0-0x9E

1-0x9C(Multi i- GPU)

PEX_PLL_EN_TERM

0-Disable

1-Enable

3GIO_PADCFG

0110-Gen1/Gen2

0000-Gen3

PCI_MAX_SPEED

0-booting to P0E Gen1

1-booting to P0E Gen2/Gen3

PCI_SPEED_CHNAGE_GEN3

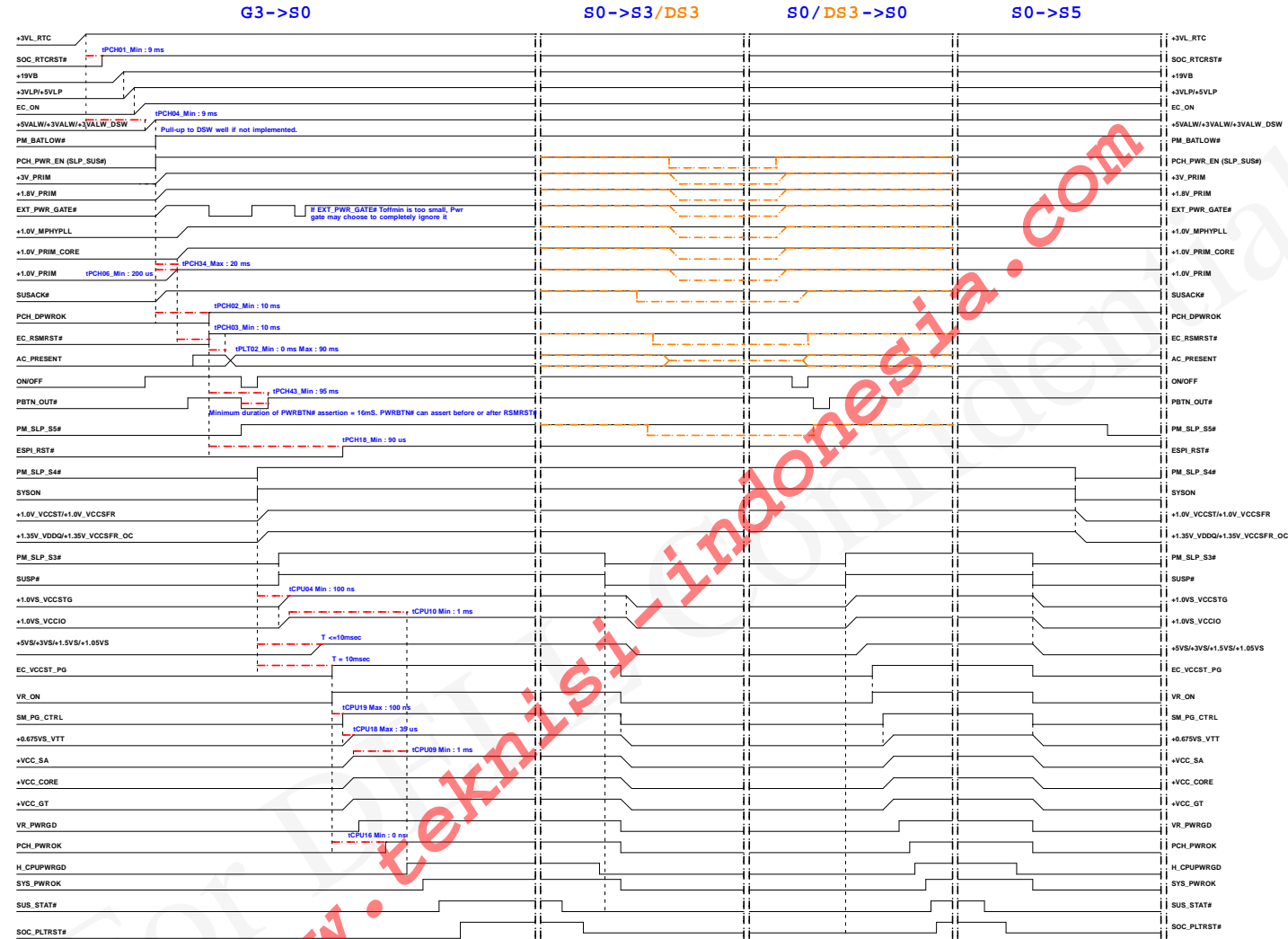
0-Disable PCIe Gen3

1-Enable PCIe Gen3

Physical Strapping pin	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	PCI_DEVICE[4]	SUB_VENDER	PCI_DEVICE[5]	PEX_PLL_EN_TERM
ROM_SO	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SI	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	3GIO_CFG[3]	3GIO_CFG[2]	3GIO_CFG[1]	3GIO_CFG[0]
STRAP2	PCI_DEVICE[3]	PCI_DEVICE[2]	PCI_DEVICE[1]	PCI_DEVICE[0]
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	RESERVED	PCI_SPEED_CHNAGE_GEN3	PCI_MAX_SPEED	DP_PLL_VDD33V

Security Classification	Compal Secret Data		Title	
Issued Date	2015/01/30	Deciphered Date	2016/12/31	
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N15P-GX (I/5) PEG & DAC				Sheet 55 of 78

[AAX06-PWR Sequence_SKL-H 4+4_DDR4_Volume_NON CS]

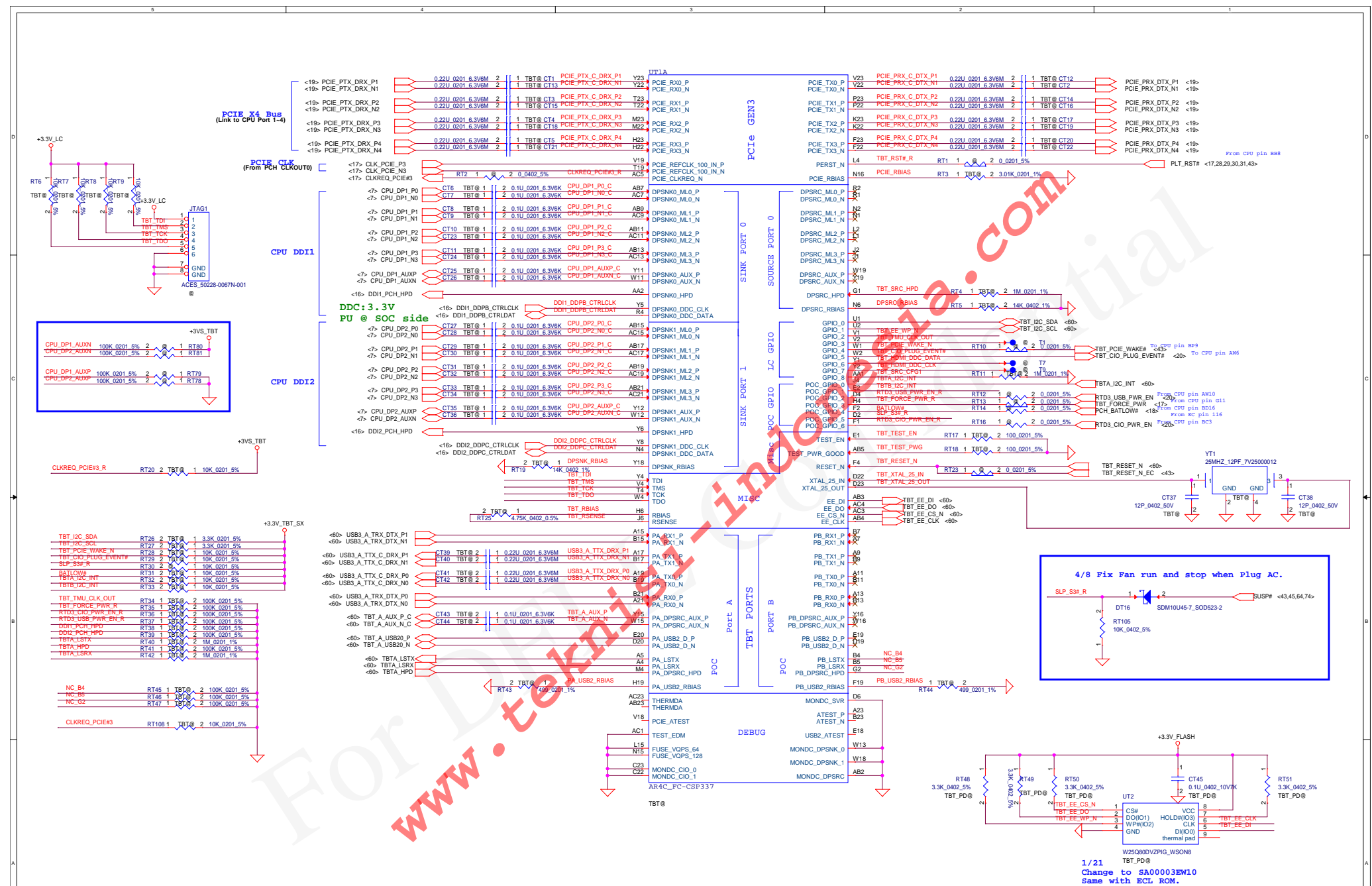


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				Doc No	LA-CV01P
				Page	1 of 1

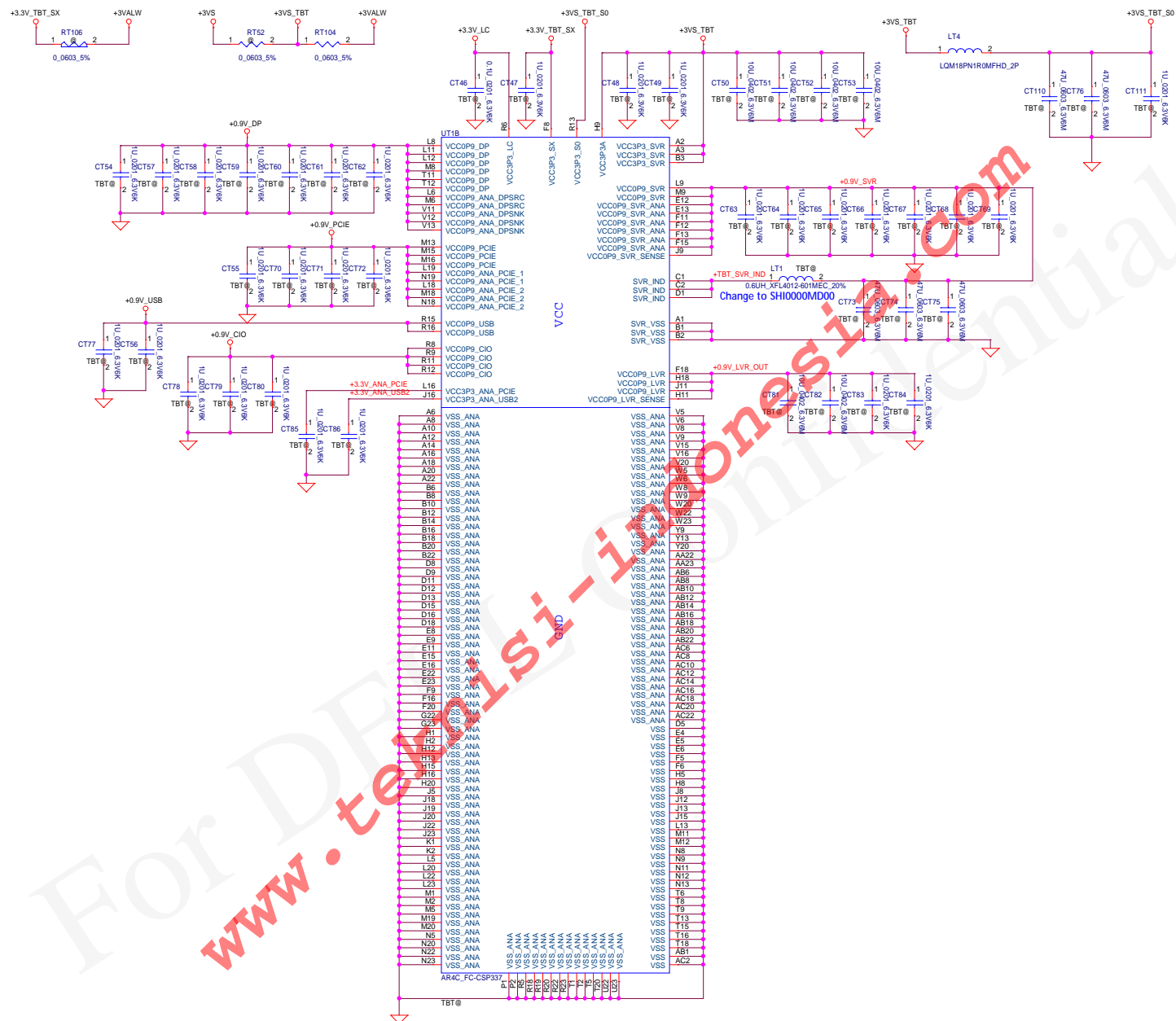
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Date: Wednesday, July 22, 2015			Sheet 67 of 78	

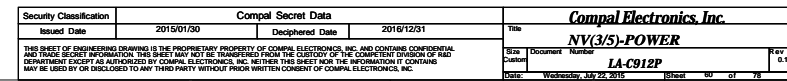


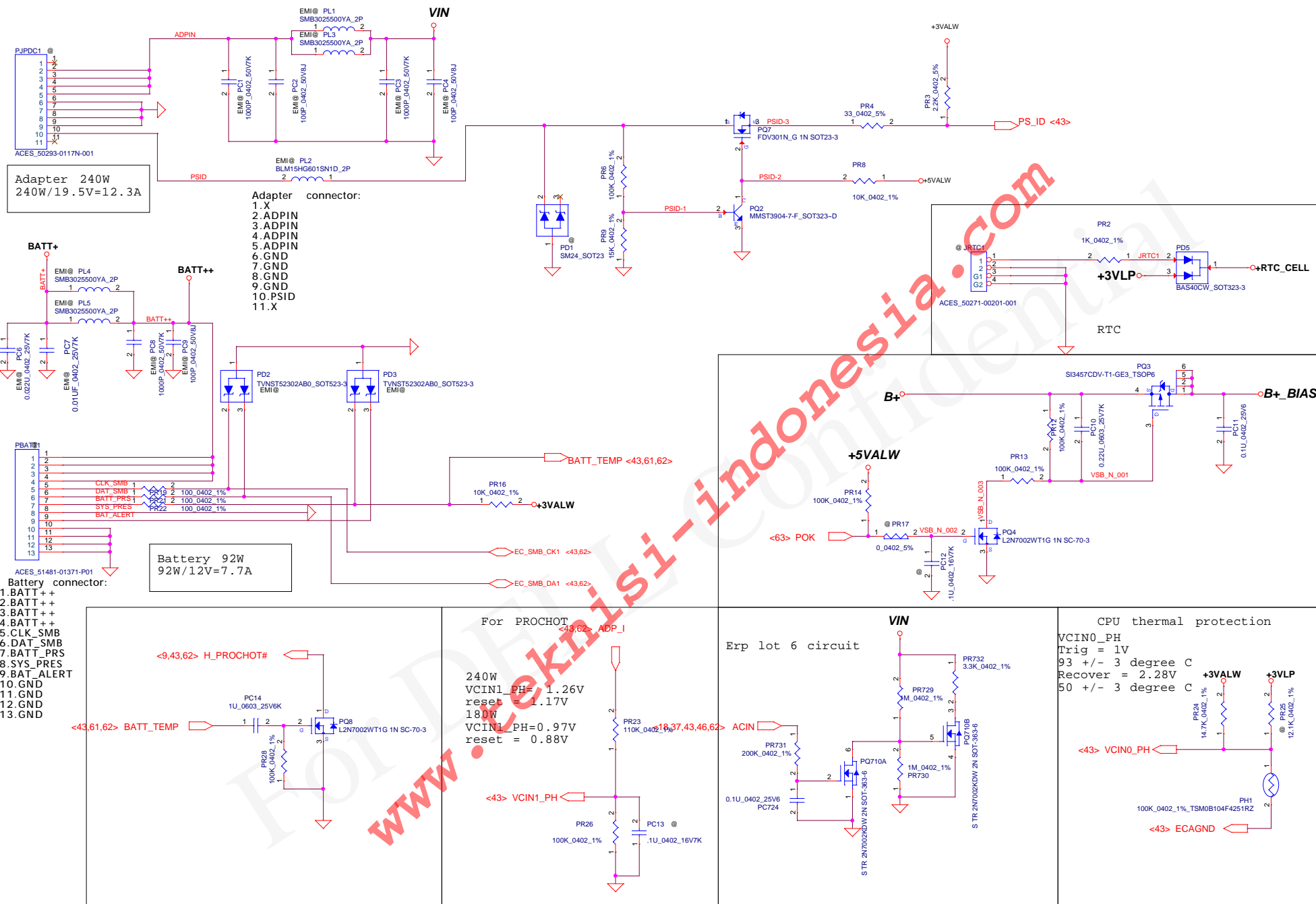
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				Custom	LA-C912P
				Date	Wednesday, July 22, 2015
				Sheet	58 of 78



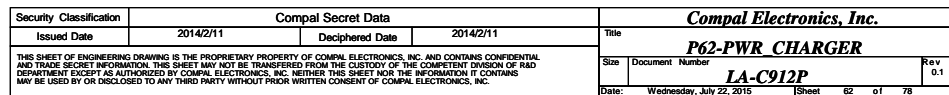
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Size		Document Number		Rev		0.1			
Custom		LA-C912P							
Date:		Wednesday, July 22, 2015		Sheet		59		of 78	

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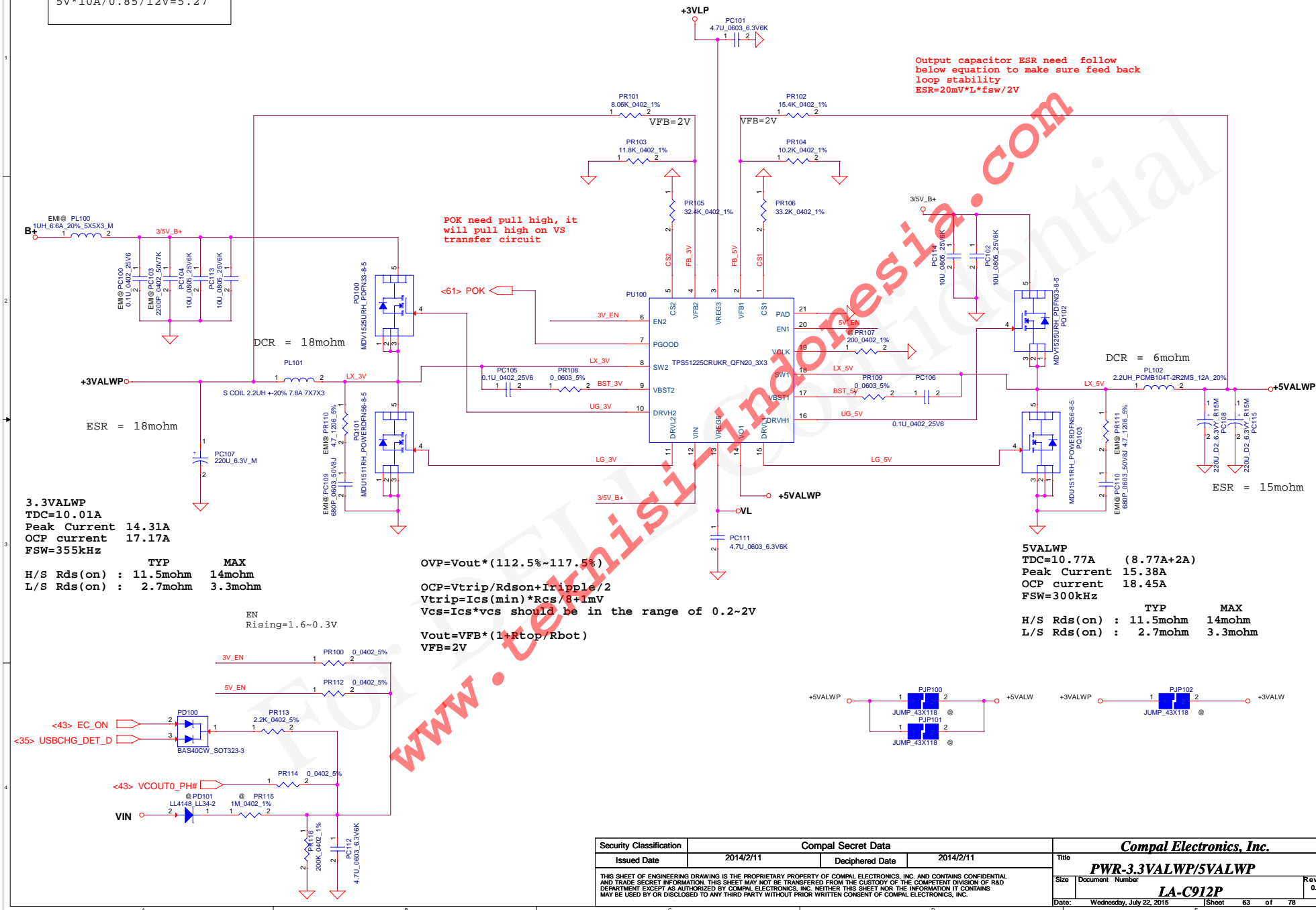




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Size		Document Number	LA-C912P	Rev 0.1
Date		Wednesday, July 22, 2015	Sheet	61 of 78

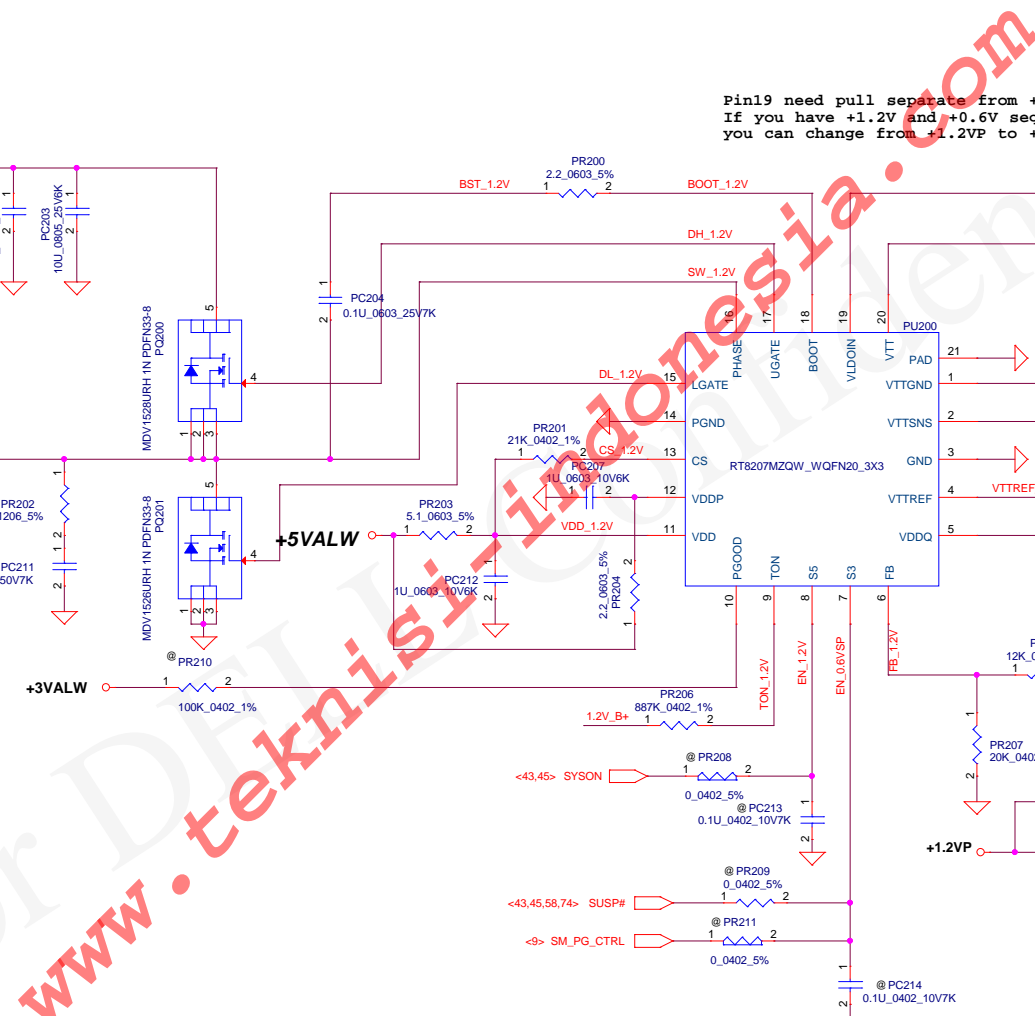


Input Current: 7.5A
 $3.3V \cdot 10A / 0.85 / 12V = 2.23$
 $5V \cdot 10A / 0.85 / 12V = 5.27$



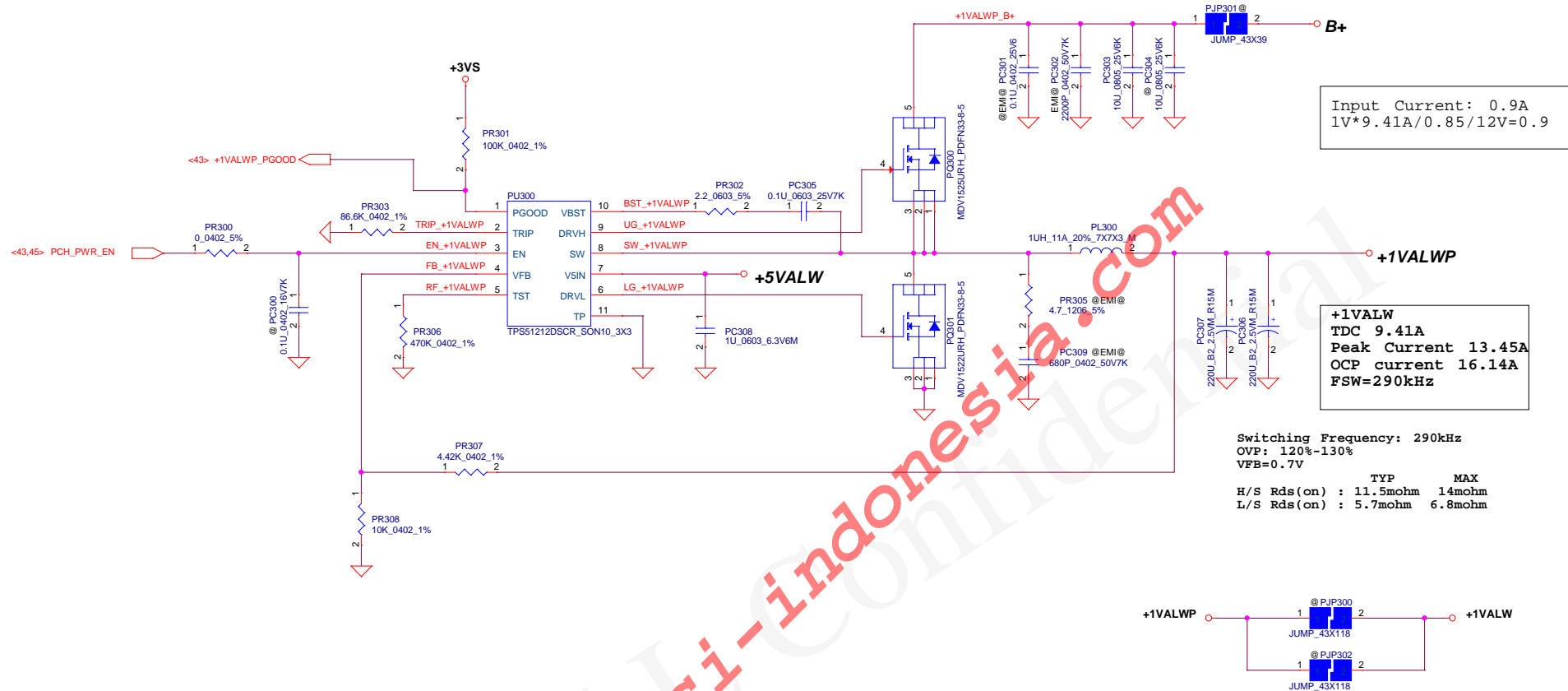
Mode	Level	+0.6VSP	VITREF_1.2V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

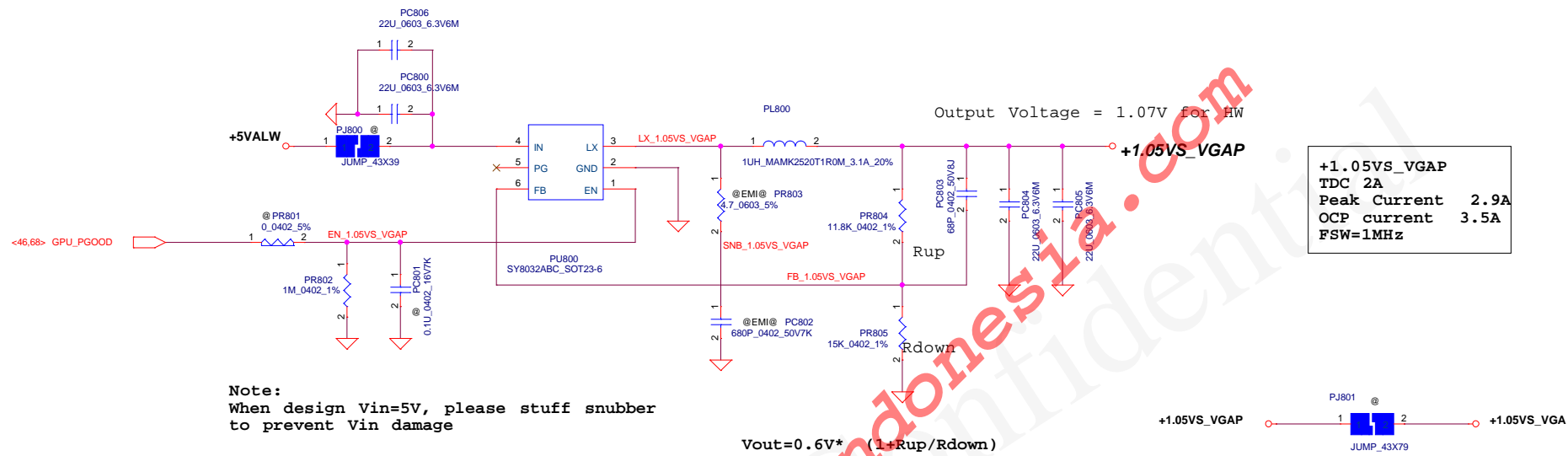


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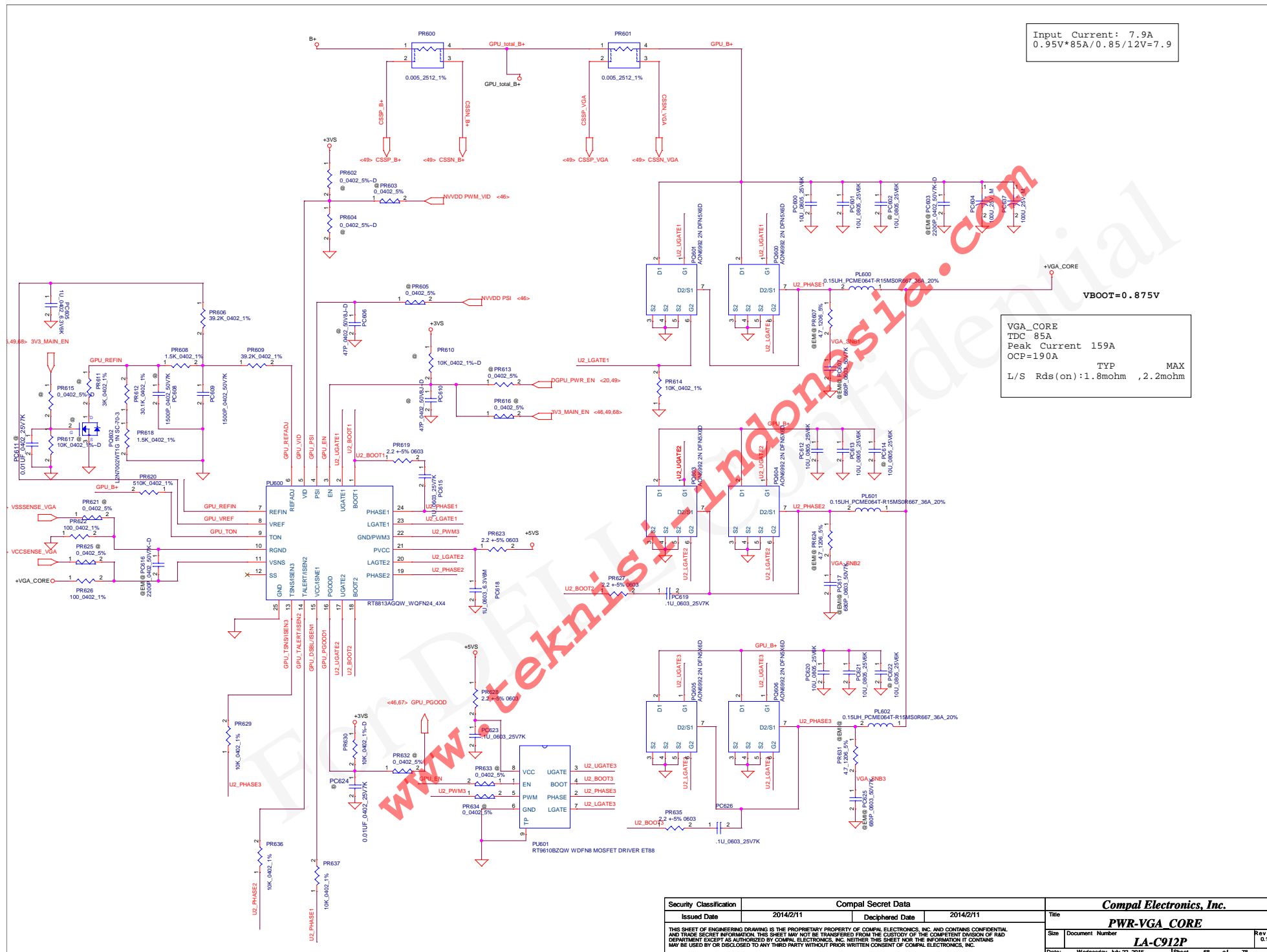


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Size		Document Number		LA-C912P		Rev 0.1
Date		Wednesday, July 22, 2015		Sheet 66		of 78



Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2014/2/11		Deciphered Date		2014/2/11		Title	
										PWR-1.05VS_VGA	
										LA-C912P	
										Rev 0.1	
										Date: Wednesday, July 22, 2015	
										Sheet 67 of 78	

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Size	Document Number	Rev
	LA-C912P	0.1
Date:	Wednesday, July 22, 2015	Sheet 69 of 78

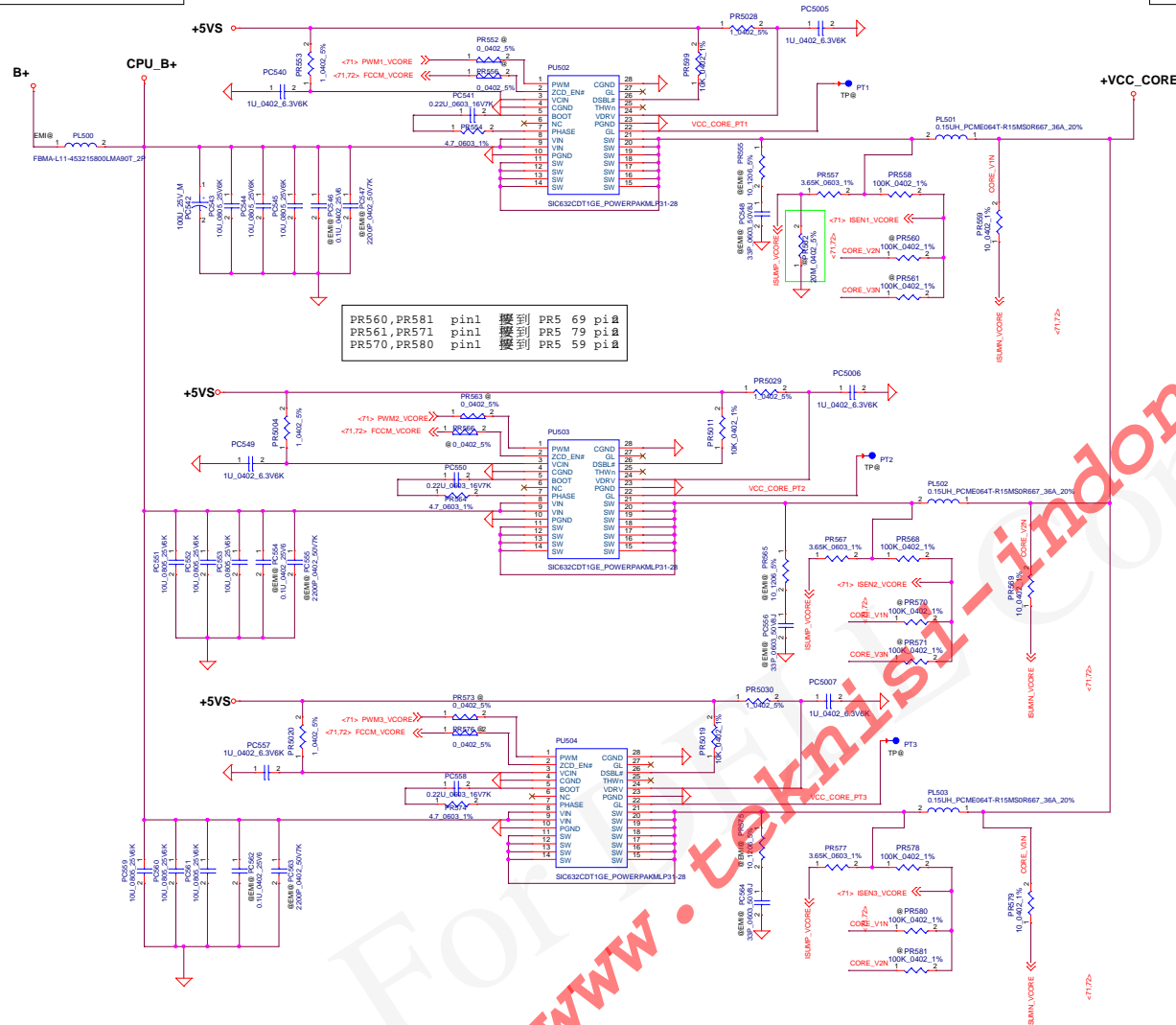


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	Compal Electronics, Inc.		
	PWR VCORE ISL95855		
	LA-C912P		
	Date: Wednesday, July 22, 2015	Sheet 71 of 78	Rev 0.1

Input Current: 8.2A
 $1.5V \times 56A / 0.85 / 12V = 8.2$

VCC_CORE
 TDC PL2 :56A
 Peak Current 68A
 OCP Current 81.6A
 DCR 0.66mohm +/-7%
 Load Line 1.8mV/A



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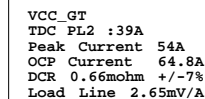


Compal Electronics, Inc.

PWR_VCORE_VCORE

LA-C912P

Rev 0.1
 Date: Wednesday, 10/22/2015
 Sheet 72 of 76



VCC_SA
TDC PL2 :10A
Peak Current 11A
OCP Current 13.2A
DCR 7.4mohm typ
Load Line 9.1mV/A

Input Current: 1.0A
$1.05V \cdot 10A / 0.85 / 12V = 1.0$

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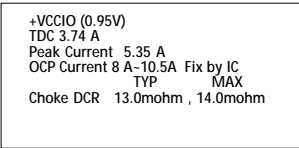
Compal Electronics, Inc.

PWR_VCORE_VGT,VSA

Number
LA-C912P

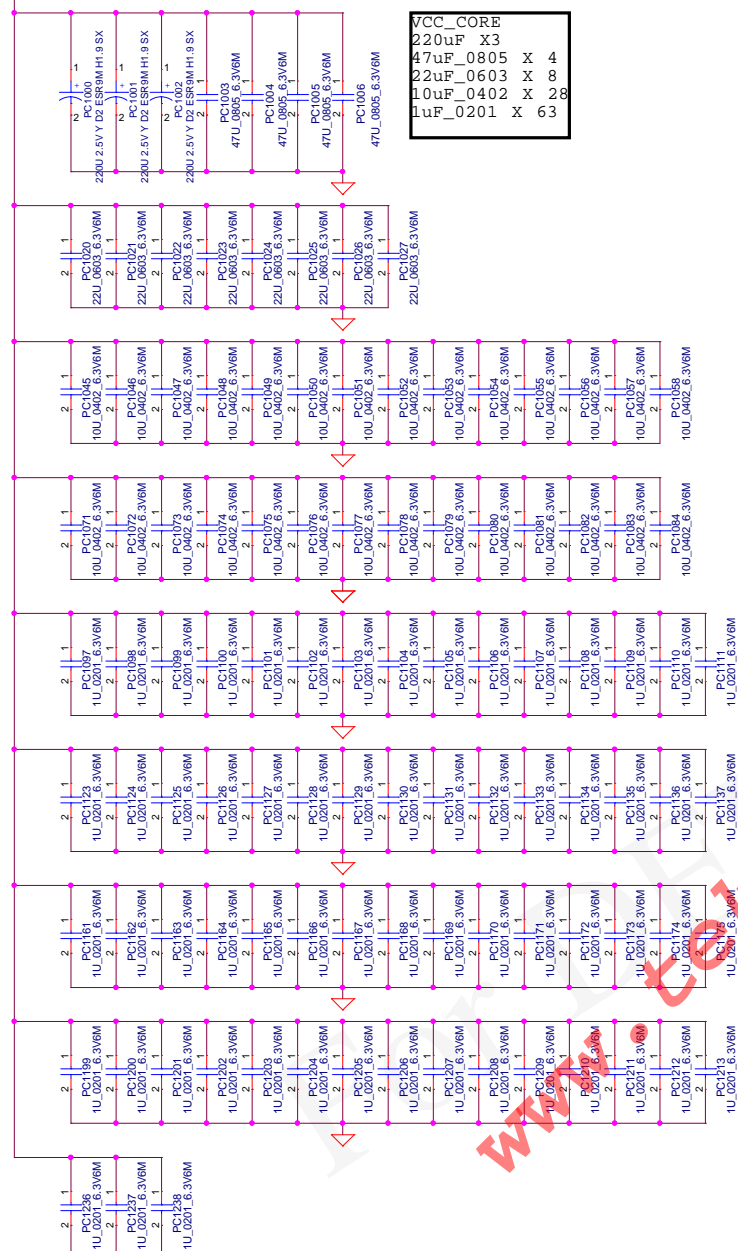
Rev	01
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Size	Document Number	Rev
	DB-1638P	0.1
Date:	Wednesday, July 22, 2015	Sheet 74 of 78

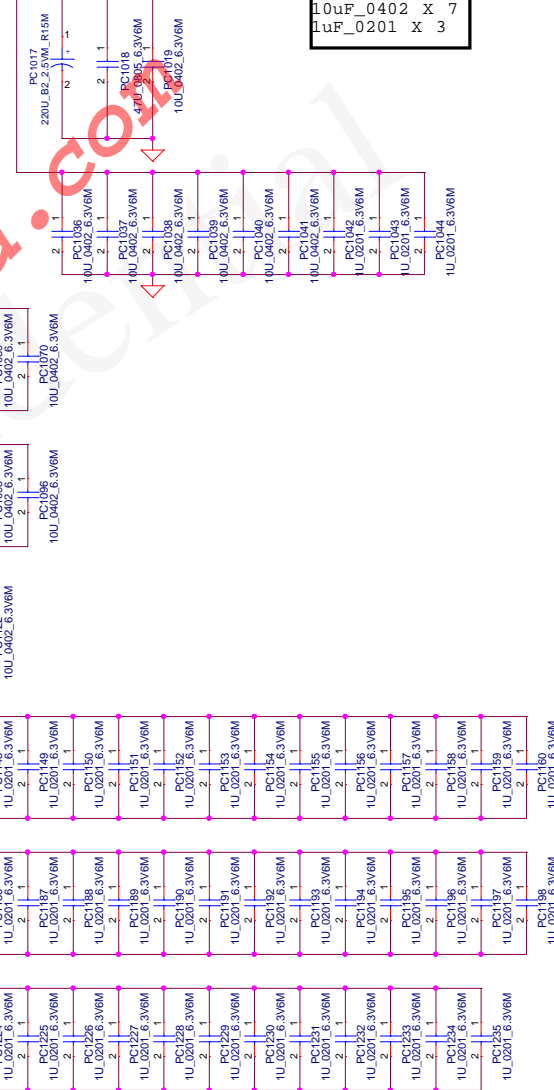
+VCC_CORE



+VCCGT



+VCCSA



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LA-C911P

Size

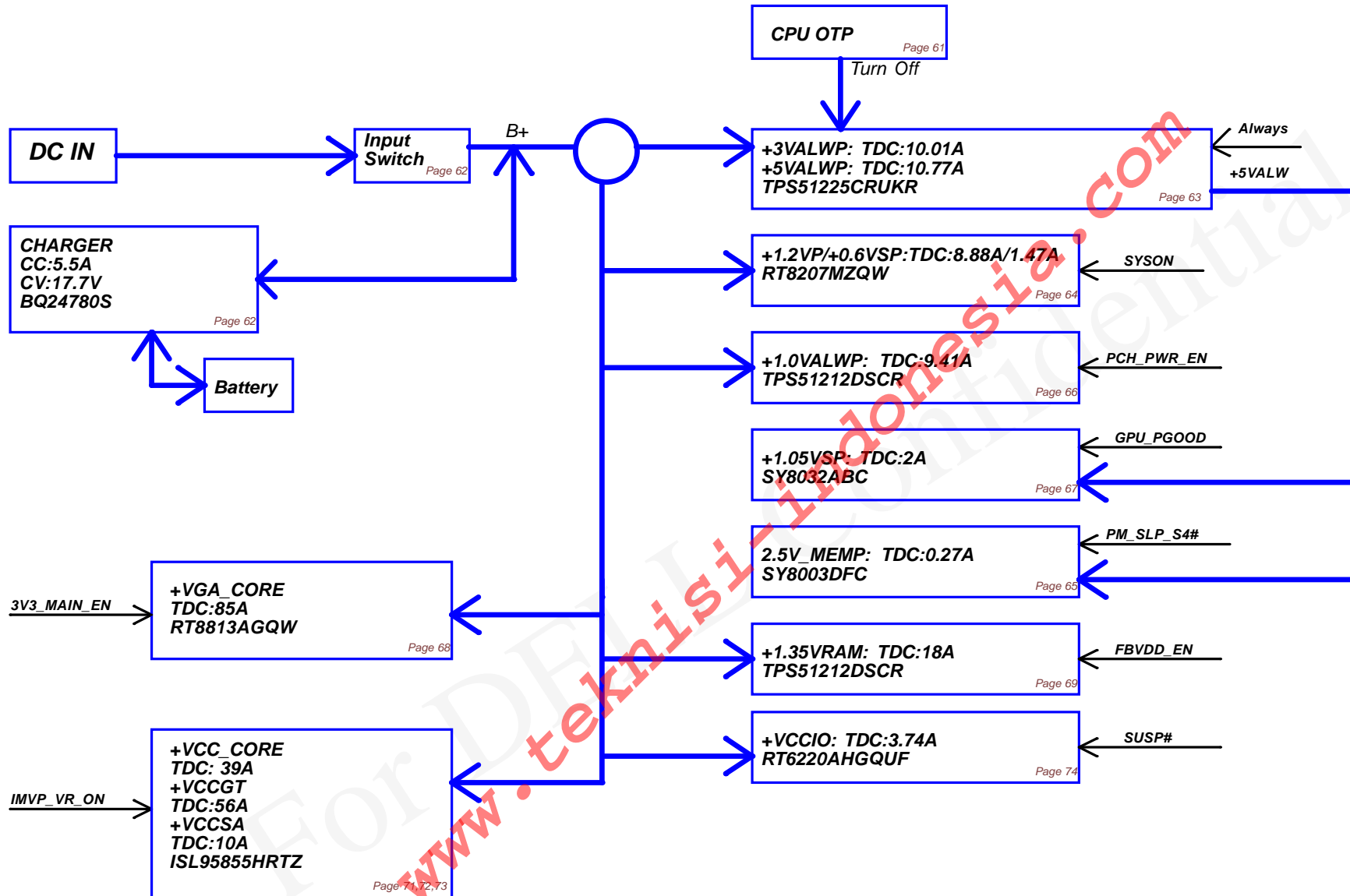
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Number

Date: Wednesday, July 22, 2015

Sheet 75 of 78

Power block



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				Size Document Number
				LA-C912P
				Rev 0.1
				Date: Wednesday, July 22, 2015
				Sheet 76 of 78

Version Change List (P. I. R. List)

Page 1

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	68	PWR_+VGA_CORE	2015.4.1	Nick_Lin	Change VGA_CORE Choke	Change from S COIL .12UH 20% PCME063T-R12MS0R625 41A (SH00000QR00) to 0.15UH_PCME064T-R15MS0R667_36A_20% (SH00000U300) Location:PL600,PL601,PL602	
2	71	PWR_VCORE_ISL95855	2015.4.1	Nick_Lin	Change net from +1.0V_VCCST to +VCCST		
3	71	PWR_VCORE_ISL95855	2015.4.1	Nick_Lin	umount PR5034,PR5035,PR5036,PR5037,PR5038,PR5039	Change from 100_0402_1% (SD034100080) to @ Location:PR5034,PR5035,PR5036,PR5037,PR5038,PR5039	
4	66	PWR_+1VALWP	2015.4.11	Nick_Lin	Change OCP setting	Change from 210K_0402_1%_0402_1% (SD034210380) to 86.6K_0402_1% (SD034866280) Location:PR303	
5	69	PWR_+1.35VRAM	2015.4.11	Nick_Lin	Mount PC627 for Acoustic	Change from 100_0805_25V (SE00000QK00) to 22U_0805_25V (SE00000XH80) Location:PC638	
6	69	PWR_+1.35VRAM	2015.4.11	Nick_Lin	Change PC630 for Acoustic	Add 22U_0805_25V (SE00000XH80) Location:PC627,PC630	
7	62	PWR_CHARGER	2015.4.11	Nick_Lin	Change PR702 for PMON function	Change from 0.004_1206_1% (SD000017Q00) to 0.005_1206_1%(SD000017R00) Location:PR303	
8	71	PWR_VCORE_ISL95855	2015.4.27	Nick_Lin	Change ISL95855 circuit by FAE advice	Change form SD000009480 (S RES 1/16W 1.47K +-1% 0402) to SD034127180 (S RES 1/16W 1.27K +-1% 0402) Location PR524 Change form SD000009M80 (S RES 1/16W 2.61K +-1% 0402) to SD00000UV00 (S RES 1/16W 3.6K +-1% 0402) Location PR530 Change form SE068221J80 (S CER CAP 220P 25V J NPO 0402) to SE074152K80 (S CER CAP 1500P 50V K X7R 0402) Location PC514 Change form SD034100180 (S RES 1/16W 1K +-1% 0402) to SD000003480 (S RES 1/16W 316 +-1% 0402) Location PR532 Change form SE074681K80 (S CER CAP 680P 50V K X7R 0402) to SE074331K80 (S CER CAP 330P 50V K X7R 0402) Location PC522 Change form SD034100180 (S RES 1/16W 1K +-1% 0402) to SD034453180 (S RES 1/16W 4.53K +-1% 0402) Location PR537 Change form SD034113380 (S RES 1/16W 113K +-1% 0402) to SD034110380 (S RES 1/16W 110K +-1% 0402) Location PR539 Change form SE075223K80 (S CER CAP 0.022U 25V K X7R 0402) to SE076333K80 (S CER CAP .033U 16V K X7R 0402) Location PC530 Change form SD034267080 (S RES 1/16W 267 +-1% 0402) to SD034301080 (S RES 1/16W 301 +-1% 0402) Location PR541 Change form SE074222K80 (S CER CAP 2200P 50V K X7R 0402) to SE074471K80 (S CER CAP 470P 50V K X7R 0402) Location PC533	

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					LA-B751P	0.1
				Date:	Wednesday, July 22, 2015	Sheet 77 of 78

Version Change List (P. I. R. List)

Page 1

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
9	71	PWR_VCORE_ISL95855	2015.4.27	Nick_Lin	Change ISL95855 circuit by FAE advice	Change form 'SD034100180 (S RES 1/16W 1K +-1% 0402) to 'SD034487100 (S RES 1/16W 4.87K +-1% 0402) Location PR511 Change form 'SE075223K80 (S CER CAP 0.022U 25V K X7R 0402) to 'SE00000MJ00 (S CER CAP 0.047U 25V K X7R 0402) Location PC517 Change form 'SE074222K80 (S CER CAP 2200P 50V K X7R 0402) to 'SE074471K80 (S CER CAP 470P 50V K X7R 0402) Location PC508 Change form 'SD034182180 (S RES 1/16W 1.82K +-1% 0402) to 'SD00000UV00 (S RES 1/16W 3.6K +-1% 0402) Location PR521 Change form 'SD034953280 (S RES 1/16W 95.3K +-1% 0402) to 'SD034976280 (S RES 1/16W 97.6K +-1% 0402) Location PR500	
10	71	PWR_VCORE_ISL95855	2015.6.24	Nick_Lin	Change VCC_CORE VR_IMAX	Change form 'SD034301080 (S RES 1/16W 301 +-1% 0402) to 'SD034442080 (S RES 1/16W 442 +-1% 0402) Location PR541 Change form 'SD034243180 (S RES 1/16W 2.43K +-1% 0402) to 'SD034357180 (S RES 1/16W 3.57K +-1% 0402) Location PR550 Change form 'SD034562180 (S RES 1/16W 5.62K +-1% 0402) to 'SD034280280 (S RES 1/16W 28K +-1% 0402) Location PR517 Change form 'SD034931280 (S RES 1/16W 93.1K +-1% 0402) to 'SD034953280 (S RES 1/16W 95.3K +-1% 0402) Location PR548	
11	71	PWR_VCORE_ISL95855	2015.6.24	Nick_Lin	Change VR_ProcHOT Trig point	Change form 'SD034105280 (S RES 1/16W 10.5K +-1% 0402) to 'SD00000AJ80 (S RES 1/16W 12.4K +-1% 0402) Location PR545,PR514	
12	61	PWR_DCIN / BATT CONN / OTP	2015.6.24	Nick_Lin	fine tune OTP setting	Change form 'SD034162280 (S RES 1/16W 16.2K +-1% 0402) to 'SD034147280 (S RES 1/16W 14.7K +-1% 0402) Location PR24	

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					LA-B751P
				Date:	Wednesday, July 22, 2015
				Sheet	78 of 78
				Rev	0.1